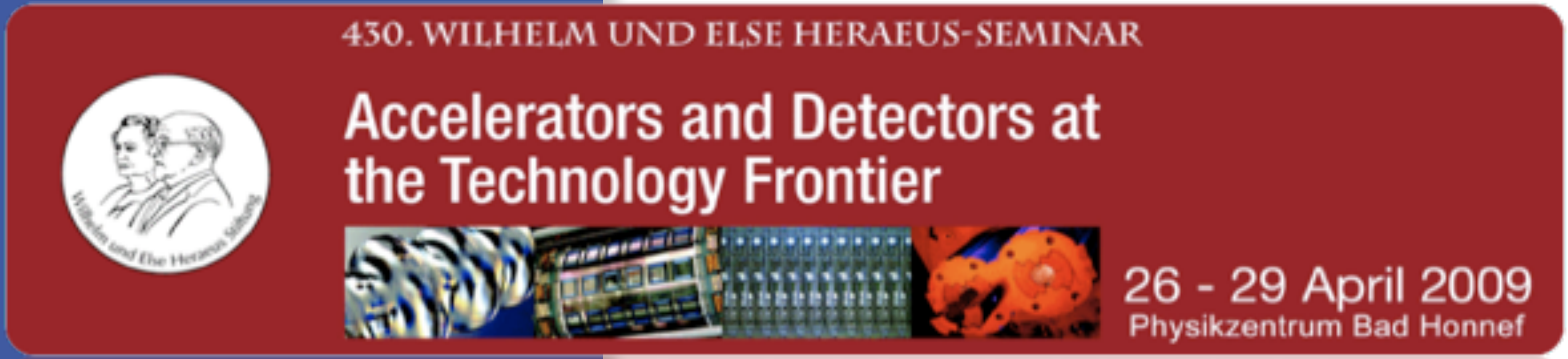
SEMICONDUCTORS AS PARTICLE DETECTORS

Ingrid-Maria Gregor, DESY



430. WILHELM UND ELSE HERAEUS-SEMINAR

Accelerators and Detectors at the Technology Frontier

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Physikzentrum Bad Honnef

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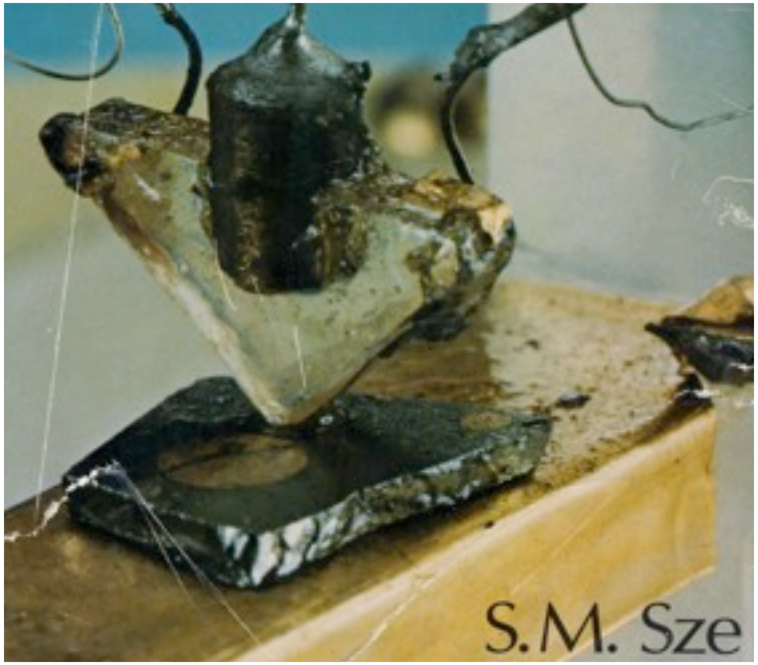
OUTLINE

- Motivation
- Basics of Semiconductor Detectors
- Strip Detectors
- Pixel Detectors
- Pixels for Future Experiments
- Summary

- Field of semiconductor detectors for particle detection is extremely large
- Can give only a rough overview
- My view is biased
  - ➔ a lot of silicon
  - ➔ more pixels than strips
  - ➔ almost only HEP



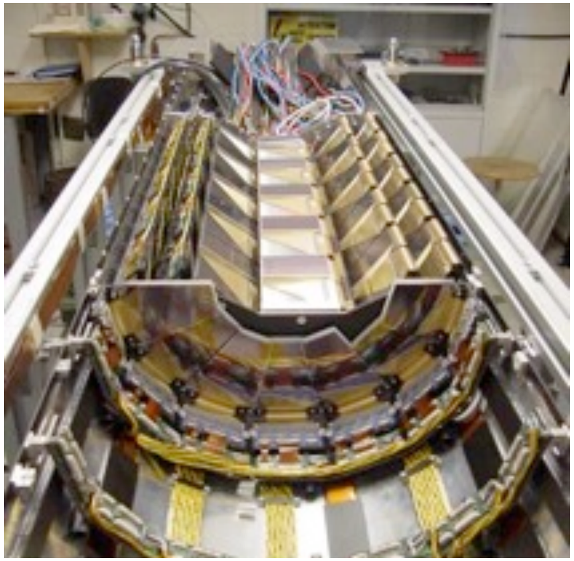
The first transistor, invented at Bell Laboratories 1947

MOTIVATION

Semiconductors have been used in particle identification for many years:

- ~1950: Discovery that pn-Junctions can be used to detect particles.
  - Semiconductor detectors used for energy measurements (Germanium)
- Since ~ 30 years: Semiconductor detectors for precise position measurements.
  - precise position measurements possible through fine segmentation (10-100µm)
  - multiplicities can be kept small (goal:<1%)

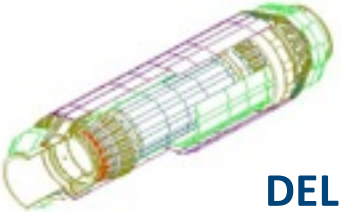
- Technological advancements in production technology:
  - developments for micro electronics



ZEUS MVD 2000

DELPHI VFT 1996

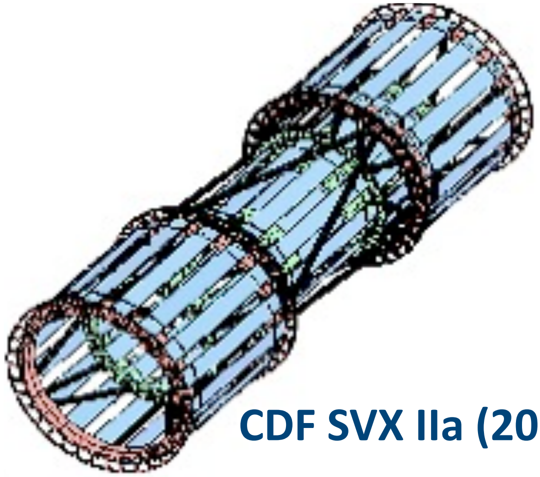
LARGE SILICON SYSTEMS



DELPHI (1996)

~ 1.8m^2 silicon area

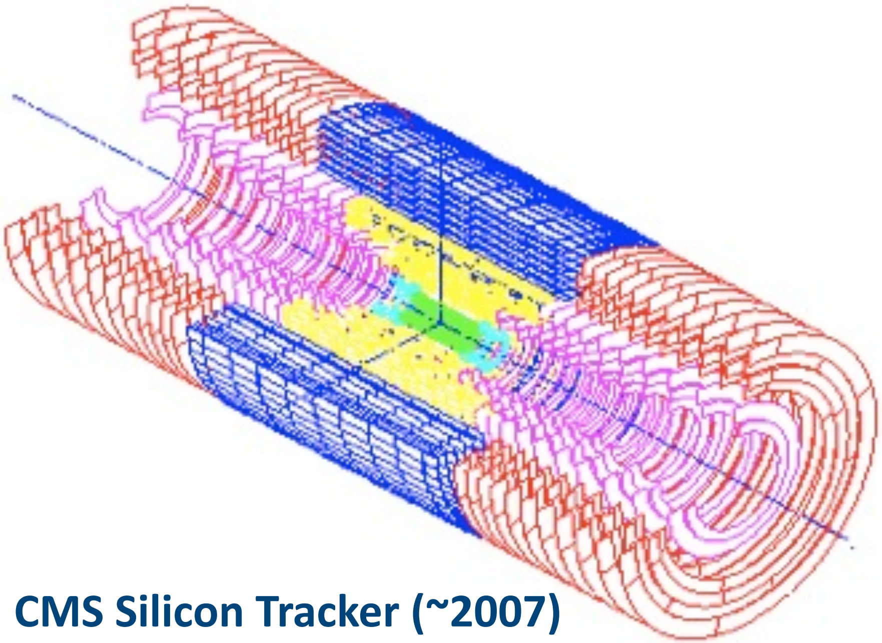
~ 175 000 readout channels



CDF SVX IIa (2001-)

~ 11m^2 silicon area

~ 750 000 readout channels



CMS Silicon Tracker (~2007)

~12,000 modules

~ 223 m^2 silicon area

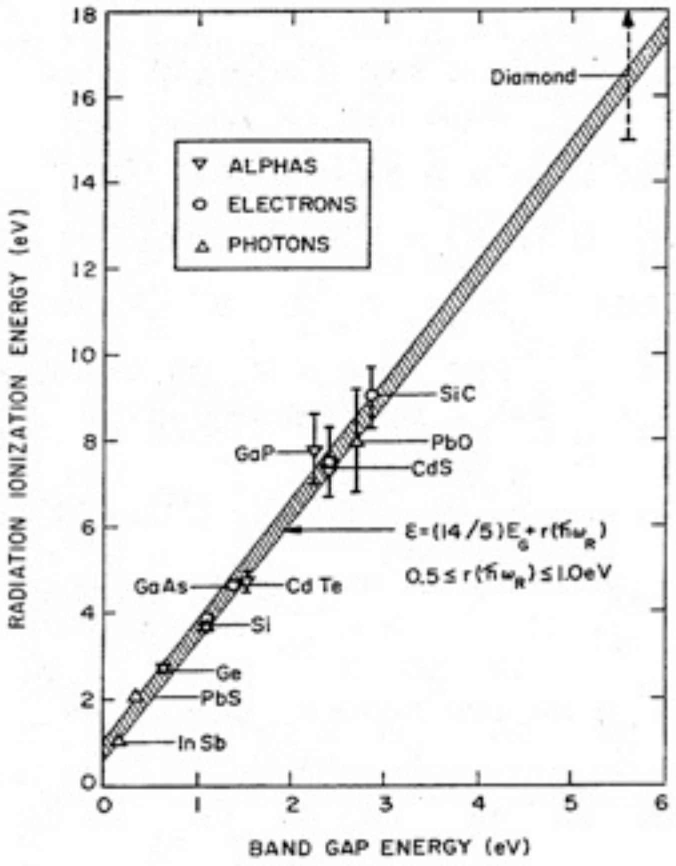
~25,000 silicon wafers

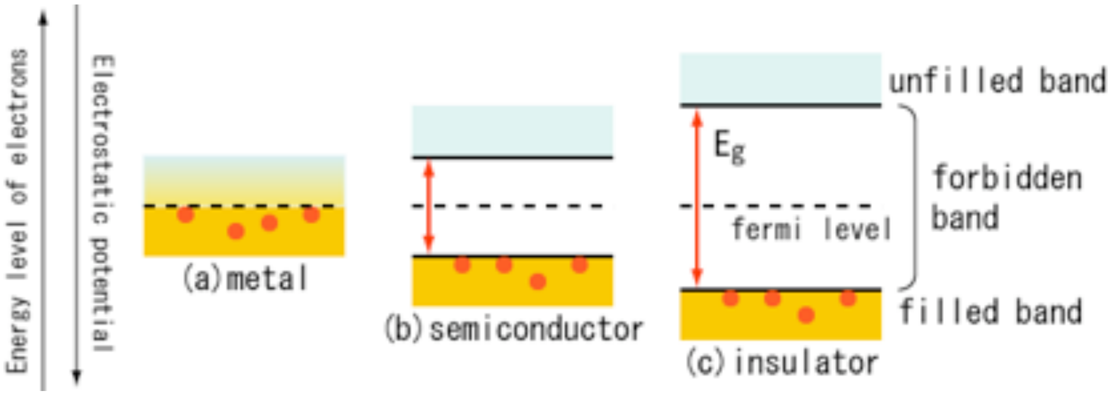
~ 10M readout channels

BASICS OF SEMICONDUCTOR DETECTORS

SEMICONDUCTOR BASICS I

- In a gas, electron energy levels are discrete.
- In a solid, energy levels split and form a nearly-continuous band.

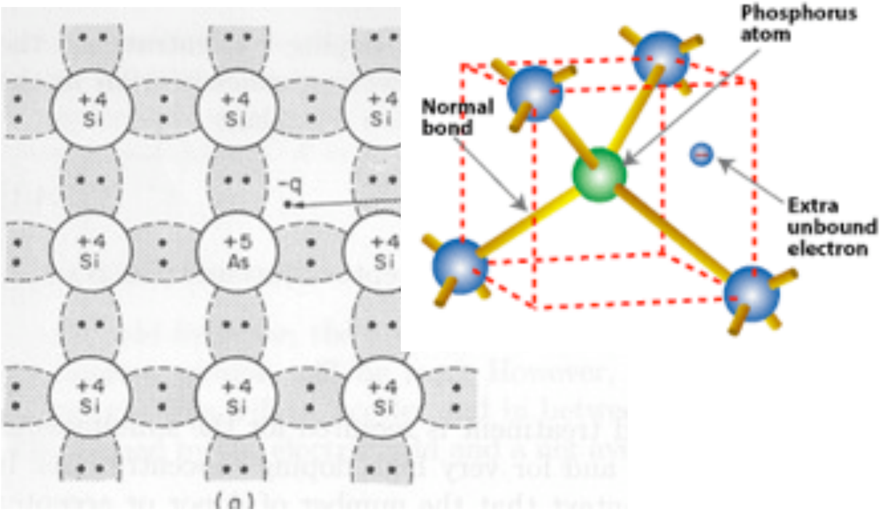


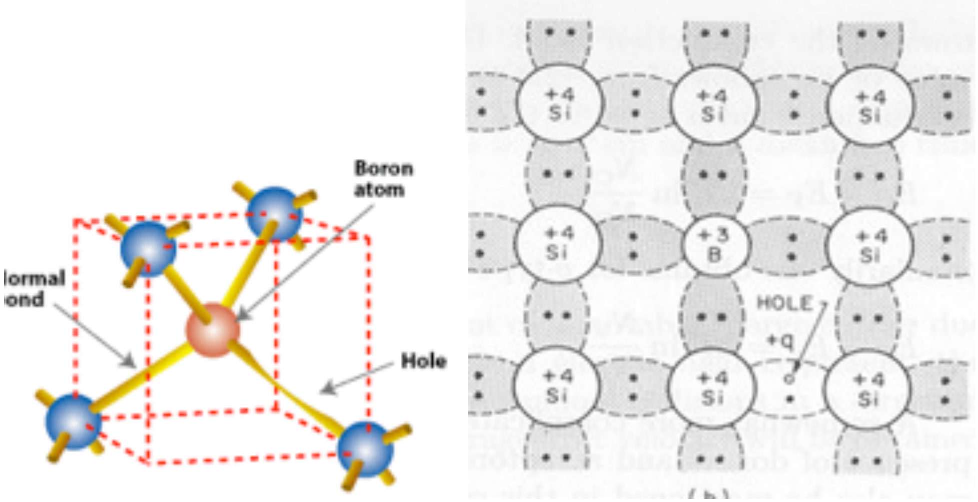


- Large gap: the solid is an insulator.
- No gap: it is a conductor.
- Small band gap: semiconductor

- For silicon, the band gap is 1.1 eV, but it takes 3.6 eV to ionize an atom. The rest of the energy goes to phonon exitations (heat).

DOPING SILICON





n-type:

- In an n-type semiconductor, negative charge carriers (electrons) are obtained by adding impurities of donor ions (eg. Phosphorus (type V))

- Donors introduce energy levels close to conduction band thus almost fully ionized => Fermi Level near CB

Electrons are the majority carriers.

p-type:

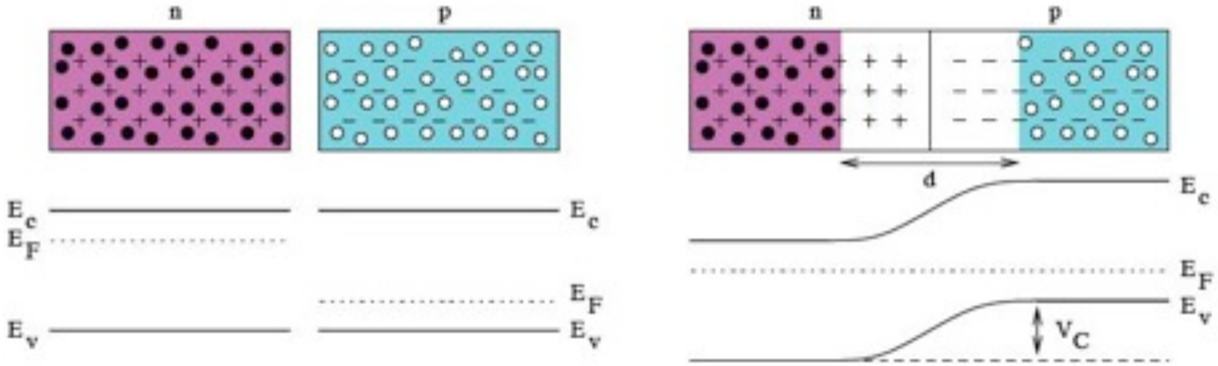
- In a p-type semiconductor, positive charge carriers (holes) are obtained by adding impurities of acceptor ions (eg. Boron (type III))

- Acceptors introduce energy levels close to valence band thus ‘absorb’ electrons from VB, creating holes => Fermi Level near VB.

Holes are the majority carriers.

PN-JUNCTION

- p- and n-doted semiconductor combined
- Gradient of electron and hole densities results in a diffuse migration of majority carriers across the junction.
- Migration leaves a region of net charge of opposite sign on each side, called the depletion region (depleted of charge carriers).



- Artificially increasing this depleted region by applying a **reversed bias voltage** allow charge collection from a larger volume

$$d = \sqrt{\frac{2\epsilon\epsilon_0 V}{e}\left(\frac{1}{n_D} + \frac{1}{n_A}\right)}$$

with $n_A >> n_D$

$$d = \sqrt{\frac{2\epsilon\epsilon_0 V}{e n_D}}$$

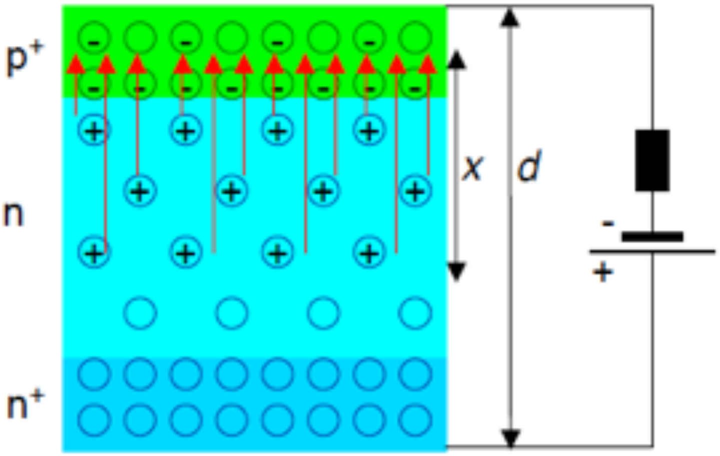
PRINCIPLE OF SEMICONDUCTOR DETECTORS

1. Creation of electric field

voltage to deplete thickness d

$$V_{\mathrm{dep}} = d^2 N_{\mathrm{eff}} \frac{q}{2\epsilon\epsilon_0}$$

N_{eff} : doping concentration



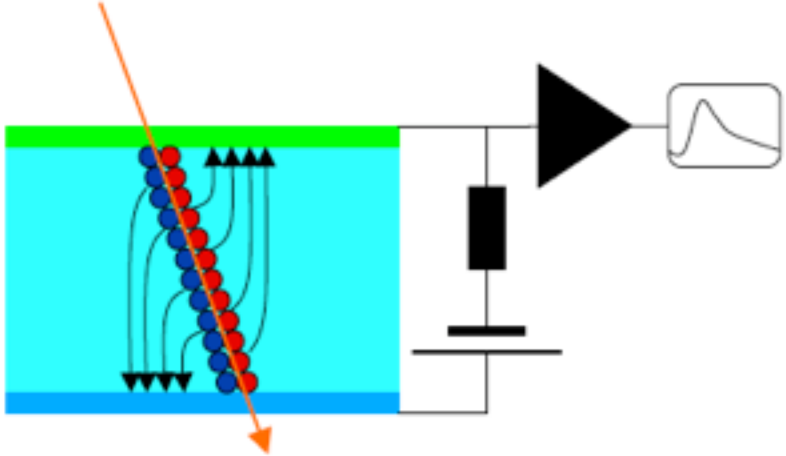
2. Keep dark current low

$$I \propto \frac{1}{\tau_g} \cdot T^2 \exp - \frac{E_g}{2kT} \times \text{volume}$$

τ_g : charge carrier life time

3. Ionising particles create free charge carrier

4. Charge carrier drift to electrodes and induce signal

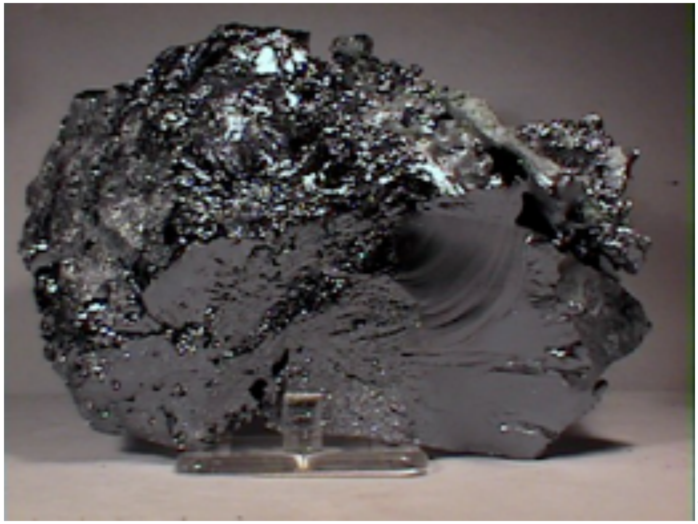


MATERIAL PROPERTIES

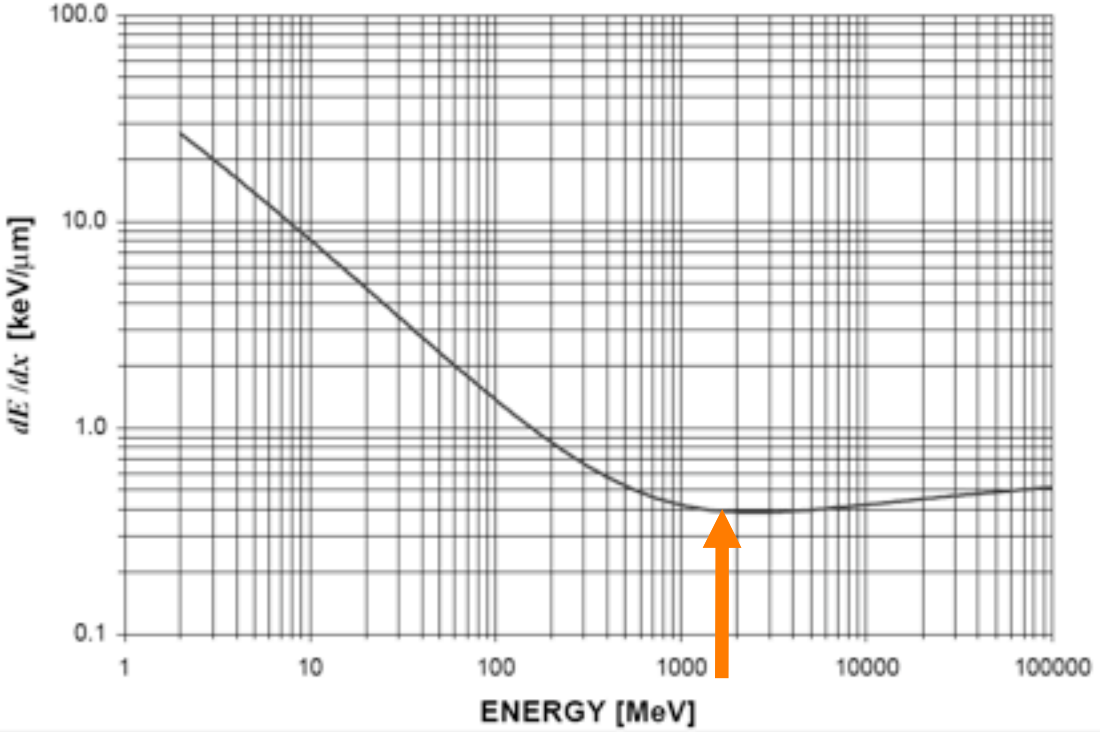
	Si	Ge	GaAs	CdTe	Diamant	SiC
band gap	1.12	0.67	1.42	1.56	5.48	2.99
energy for e-p pair [eV]	3.6	2.9	4.2	4.7	13.1	6.9
e- for MIP (300μm)	24000	50000	35000	35000	9300	19000
Z	14	32	31+33	48+52	6	14+6

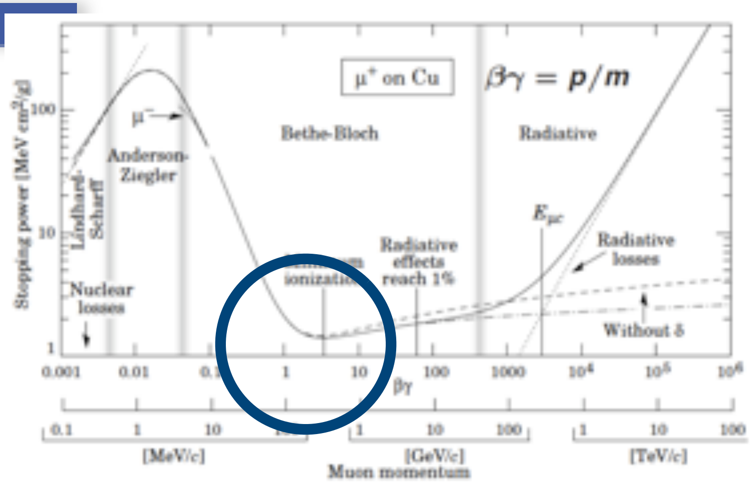
Why is silicon used more often ?

- Silicon is the only material which can be produced in larger wafers in high quality
- compare to kT = 0.026 eV at room temperature -> dark current under control
- high density compared to gases: ρ=2.33g/cm^3
- good mechanical stability -> possible to produce mechanically stable layers
- large charge carrier mobility
- fast charge collection δt~10ns

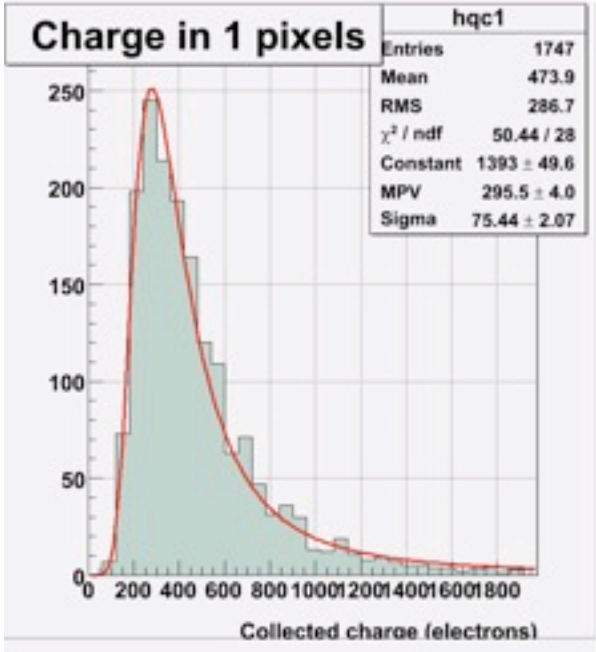


PROTONS IN SILICON



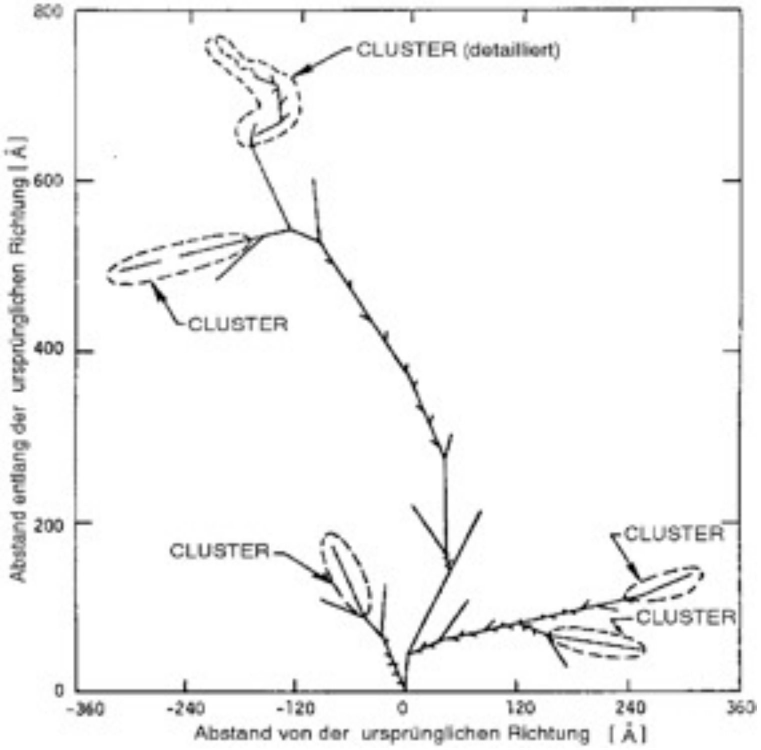


- 0.4 keV/μm
- -> 3.6 eV creates electron hole pair
- => ~110 electron-hole pairs per μm (mean value)
- most probably number: 80 electrons



RADIATION DAMAGE

- Impact of Radiation on Silicon:
- Silicon Atoms can be displaced from their lattice position
- Point defects (EM Radiation)
- Damage clusters (Nuclear Reactions)
- Important in this context:
  - Bulk Effects: Lattice damage: Generation of vacancies and interstitial atoms (NIEL: Non Ionizing Energy Loss)
  - Surface effects: Generation of charge traps (Oxides) (by ionizing energy loss)



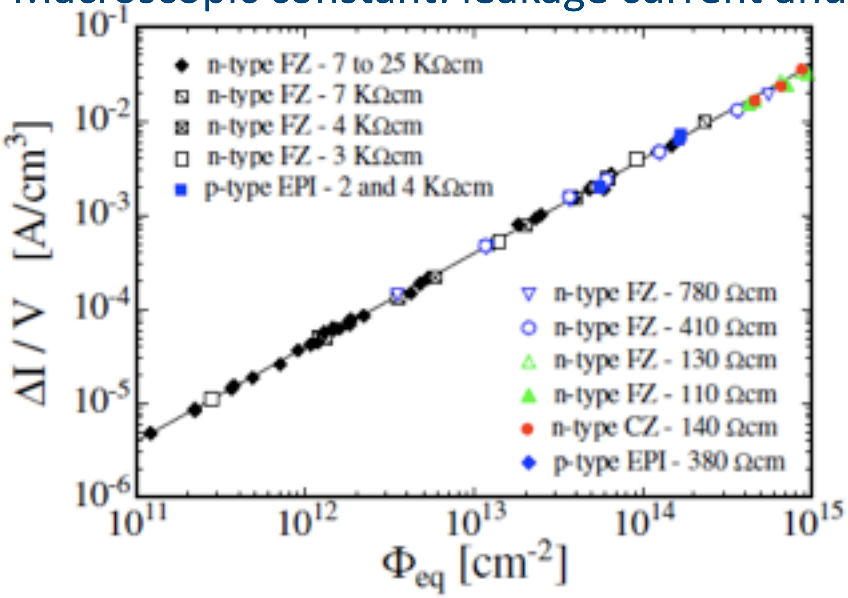
Filling of energy levels in the band gap

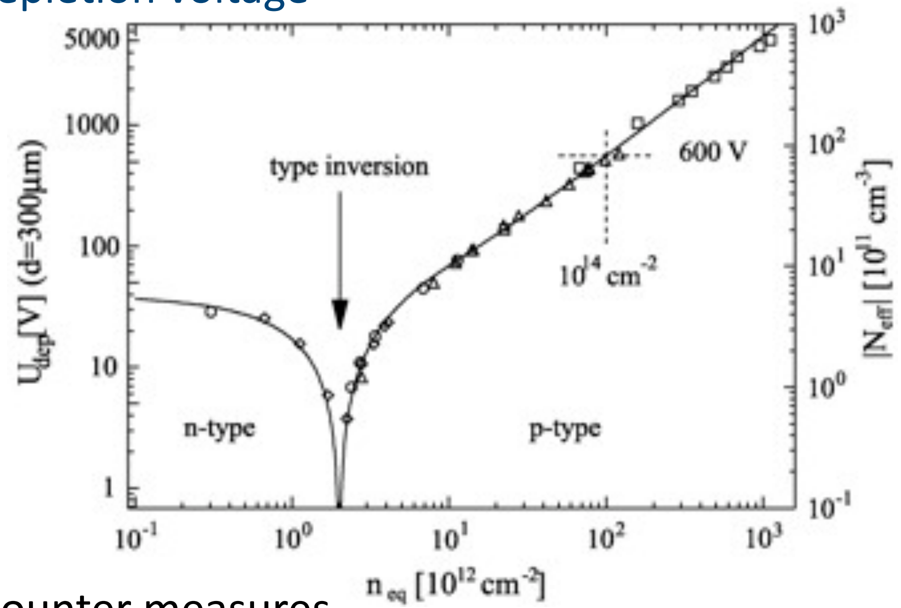
➪ direct excitation now possible
➪ higher leakage current
➪ more noise
➪ “Charge trapping”, causing lower charge collection efficiency

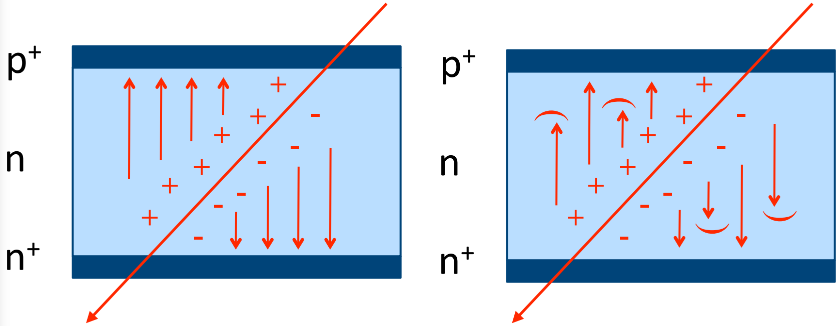
Can also contribute to space charge: Higher bias voltage necessary.

CONSEQUENCES OF RADIATION DAMAGE

Macroscopic constant: leakage current and depletion voltage







Charge trapping in defects

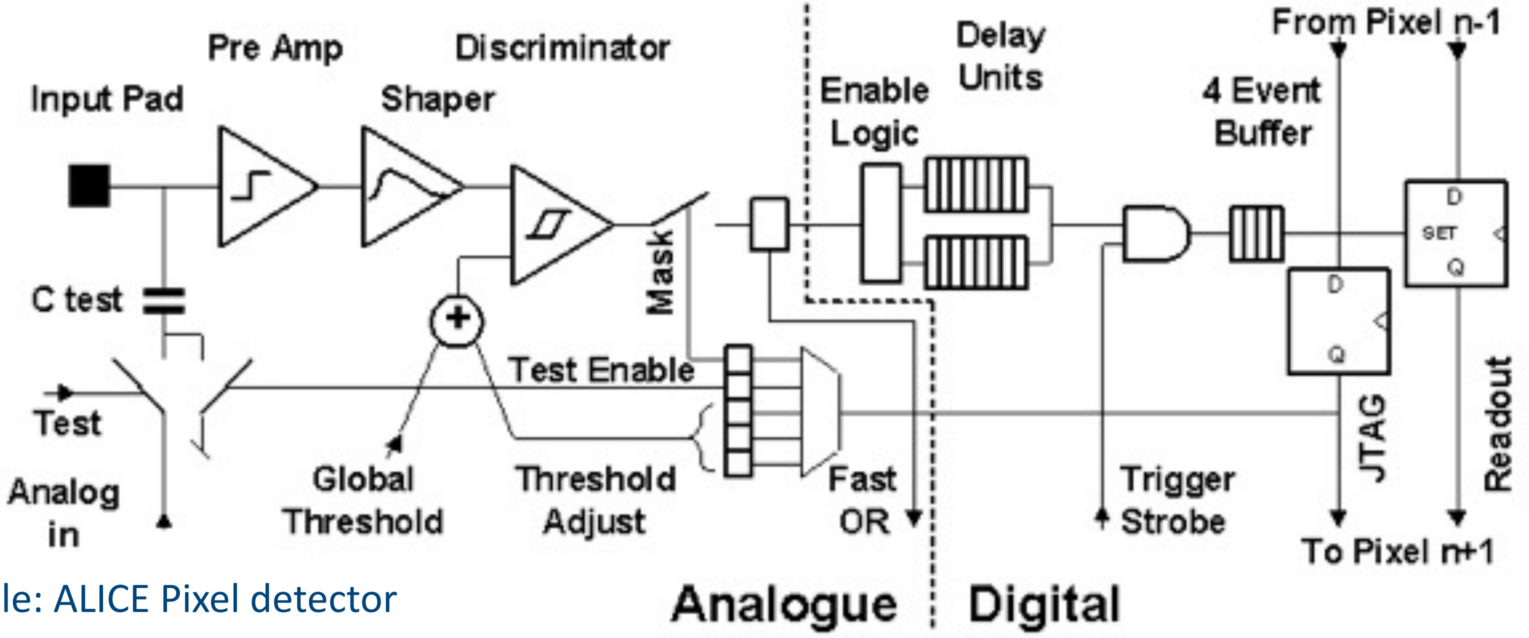
Counter measures

- Geometrical: develop sensors that can withstand higher depletion voltages
- Thinner sensors (but FE electronics with higher sensitivity needed)
- Environment: sensor cooling (~-10 C)
- Slowing down of “reverse annealing”
- Lower leakage currents

SOME WORDS ON FRONT-END ELECTRONICS

Overview of readout electronics

- Most front-ends follow a similar architecture



example: ALICE Pixel detector

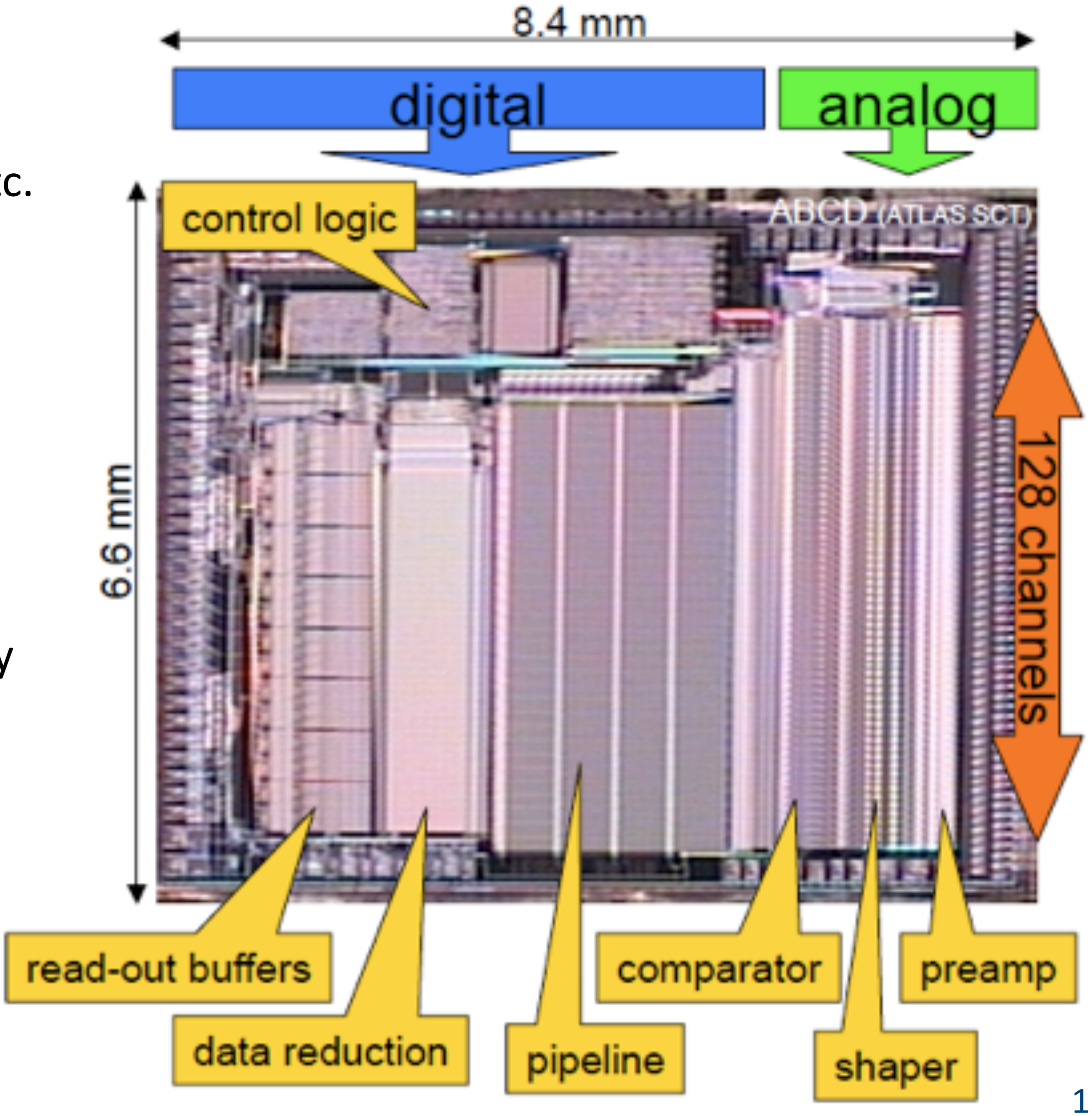
- Very small signals (fC) -> need amplification
- Measurement of amplitude and/or time (ADCs, discriminators, TDCs)
- Several thousands to millions of channels

VERY LARGE SCALE INTEGRATION

- VLSI enables
  - high channel density
  - pre-amplification, data storage etc. very close to the detector
  - reduced noise
  - low power dissipation

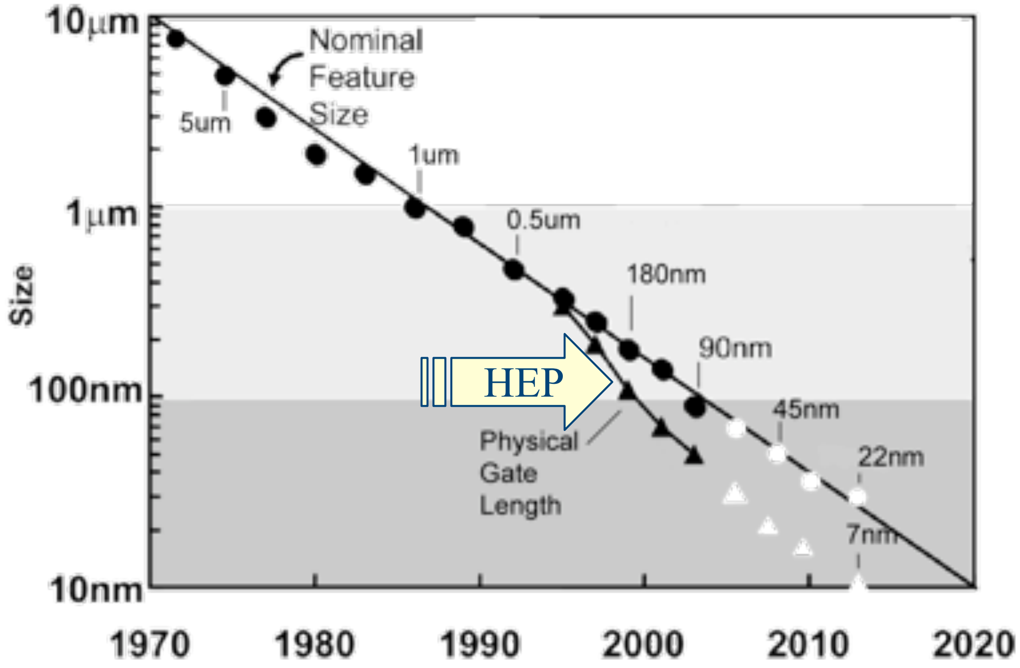
  - industrial production

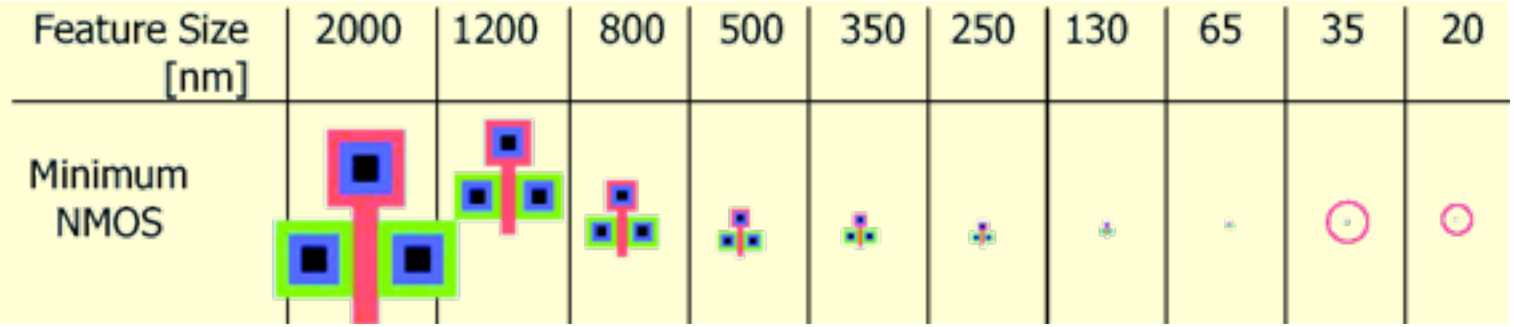
- integration density is growing rapidly



INDUSTRY SCALING ROADMAP

- New generation every ~2 years with $\alpha = \sqrt{2}$
- from 1970 (8 μm) to 2009 (35 nm) (industrial application)
- End of the road ? Power dissipation sets limits
- HEP nowadays at 90nm and 130nm
- Problem: by the time a technology is ready for HEP -> “old” in industry standards





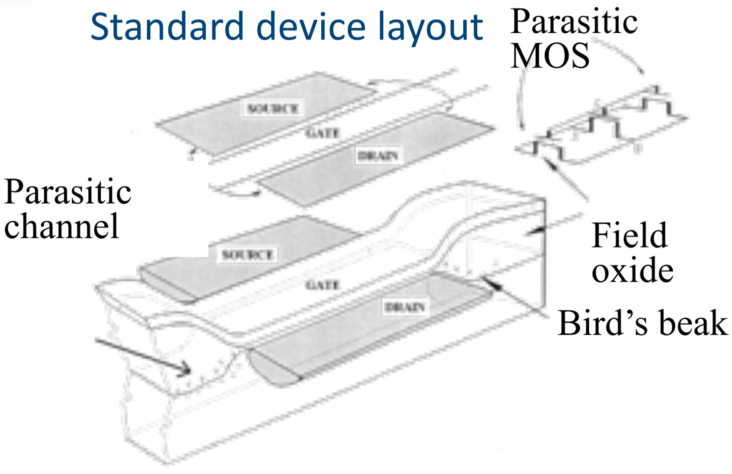
Feature Size [nm]	2000	1200	800	500	350	250	130	65	35	20
Minimum NMOS										

RADIATION EFFECTS ON CMOS: IONIZING

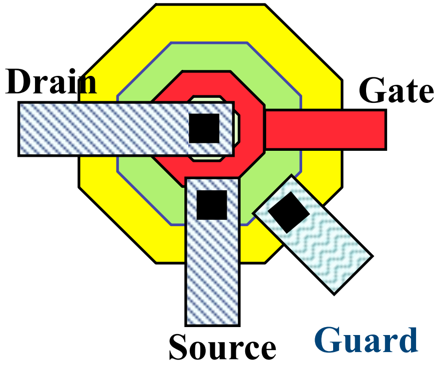
- Decrease of feature size: higher radiation tolerance:
  - Positive charge trapped in gate and field oxides
  - Trapped charge dissipates by tunnelling in thin-oxide transistors

- Radiation tolerant layout techniques designed by CERN RD49 in 0.25µm to avoid parasitic transistor leakage

Standard device layout

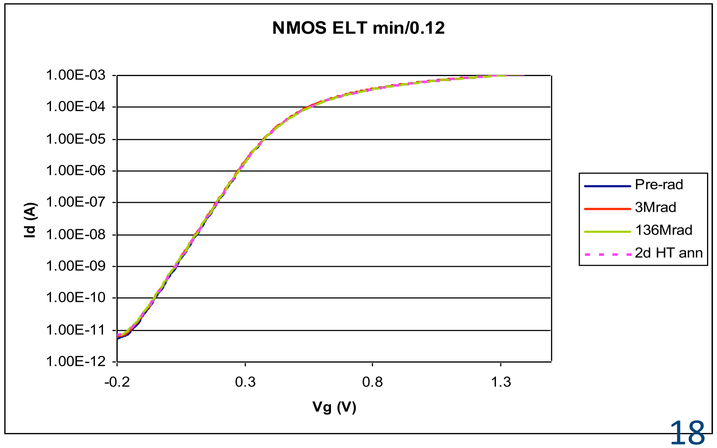


Enclosed layout



- gate encloses all n+ regions avoiding any thick transistor relevant oxide structures

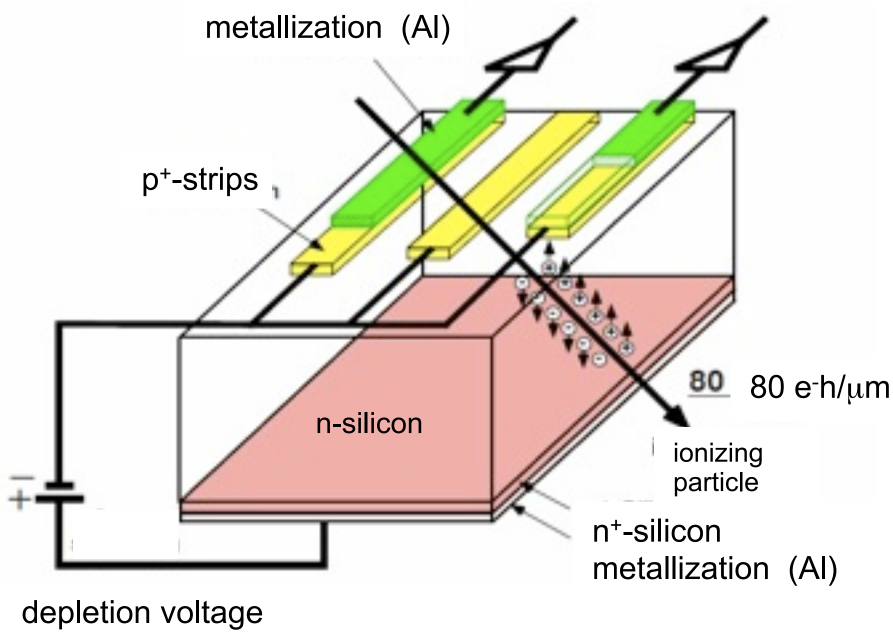
TID on IBM 130nm NMOS [F. Faccio CERN]



STRIP DETECTORS

STRIP DETECTORS

- First detector devices using the lithographic capabilities of microelectronics
- First Silicon detectors -> strip detectors
- Can be found in all high energy physics experiments of the last 20 years



Principal: Silicon strip detector

- Arrangement of strip implants acting as charge collecting electrodes.
- Placed on a low doped fully depleted silicon wafer these implants form a one-dimensional array of diodes
- By connecting each of the metalized strips to a charge sensitive amplifier a position sensitive detector is built.
- Two dimensional position measurements can be achieved by applying an additional strip like doping on the wafer backside (double sided technology)

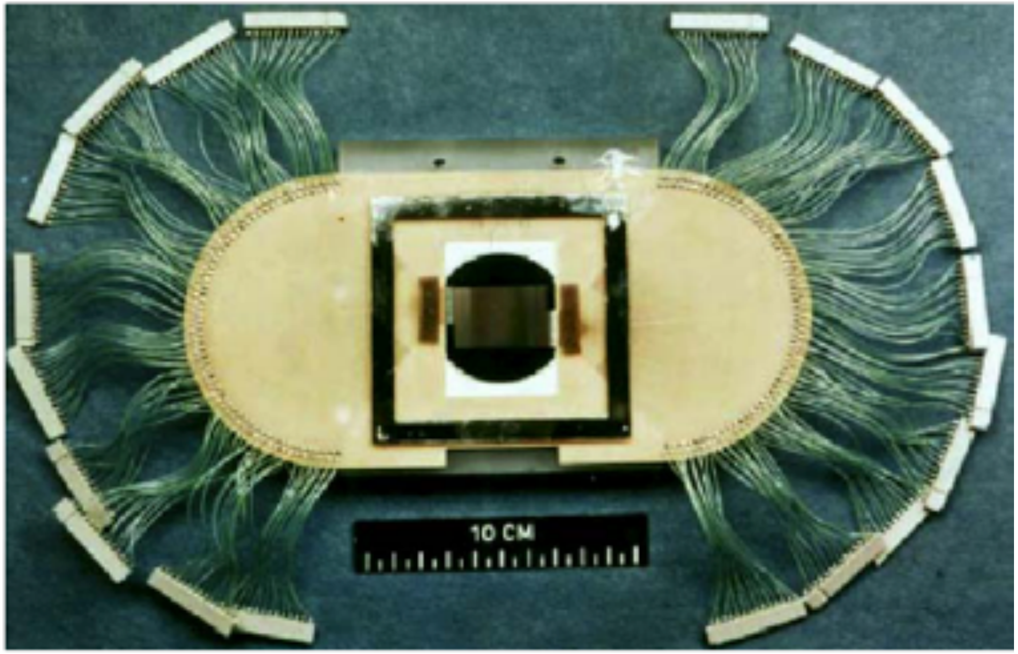
FIRST HEP APPLICATION: NA11

- After discovery of charm (1974), τ-lepton (1975) and beauty (1977) with lifetimes cτ ~100 µm: need fast (ns), and precise (µm) electronic tracking detectors

- strip detector for NA11 in 1981
  - 1200 strip-diodes
  - 20 µm pitch
  - 60 µm readout pitch
  - 24 x 36 mm^2 active area ~0.01m^2
  - position resolution ~5.4 µm
  - 8 layer at the start

  ➔ precise track reconstruction

- readout electronic: ~1m^2!



Si Microstrip Detectors for LHC

Early 1990's: At the time of the Conceptual Design of the pp Experiments

- Radiation damage poorly understood
- Cost/unit area was prohibitively large
- Large no. of channels required

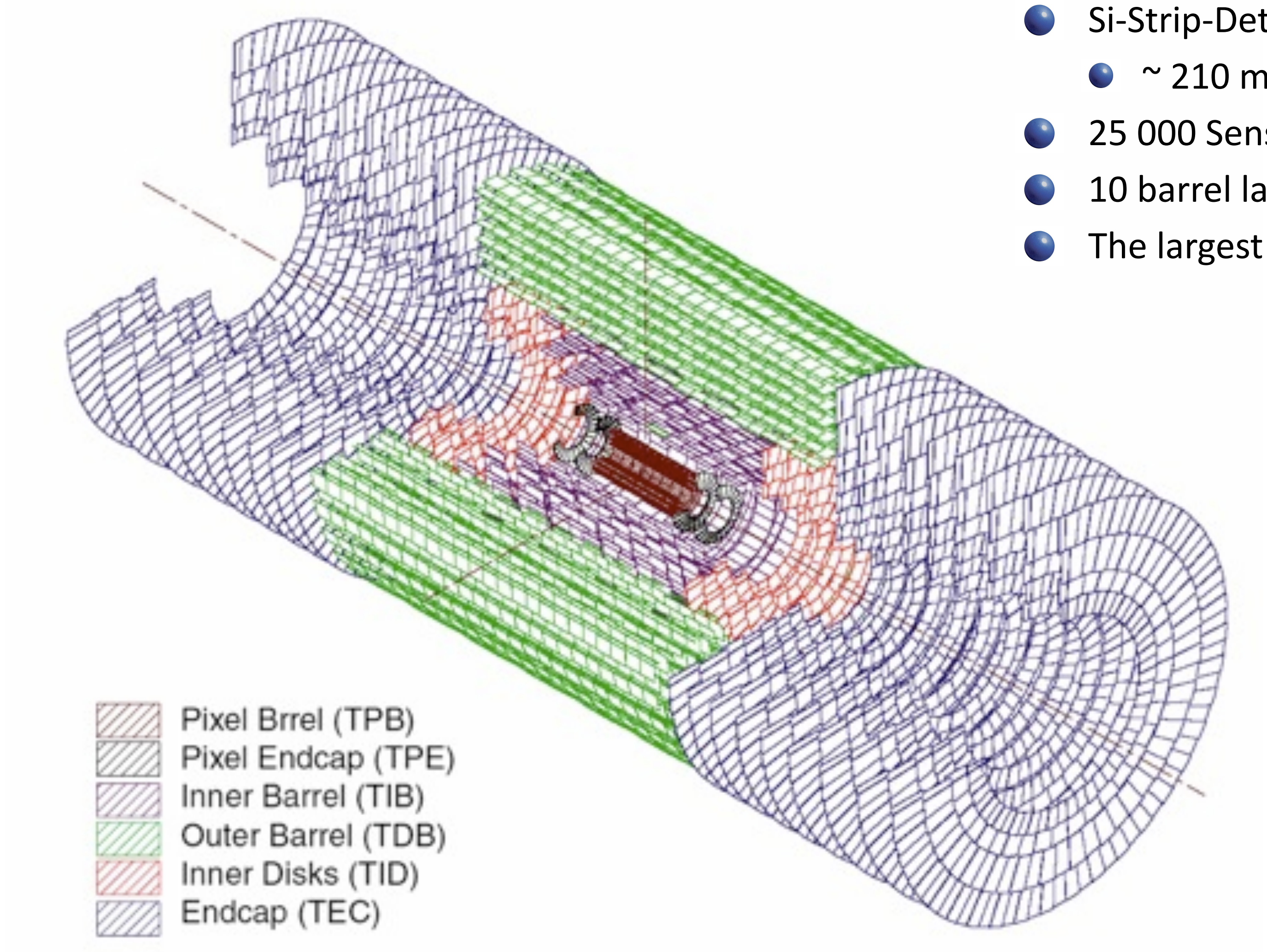
What was known :

- leakage current increased linearly with fluence
- type inversion – higher and higher bias voltage required
- reverse annealing

What was done

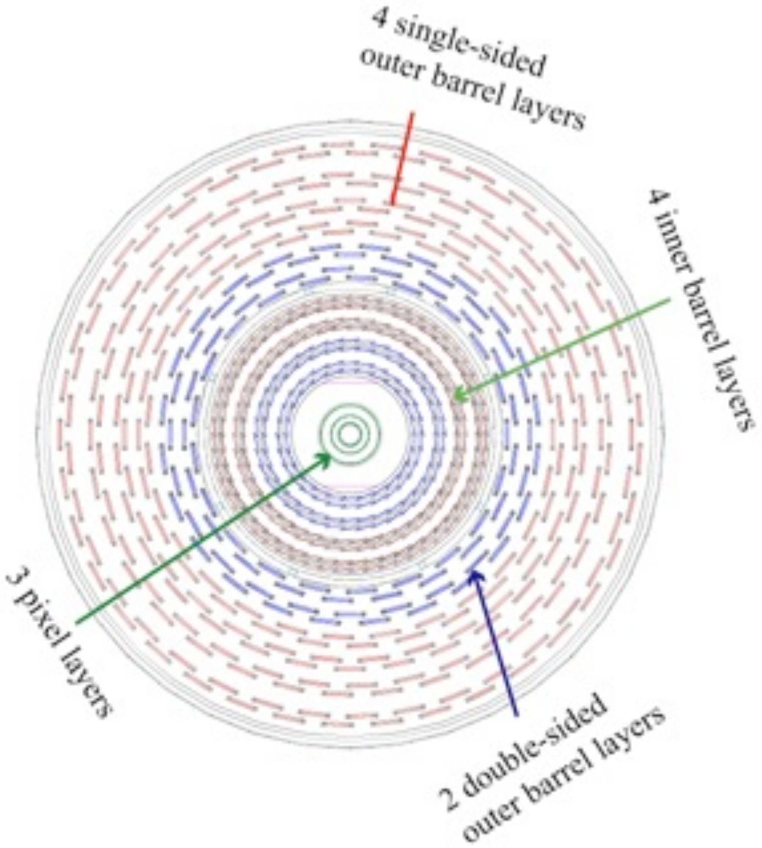
- HV behaviour improved by careful processing and use of multiple guard rings
- Si detectors had to be kept permanently cold
- Fast pre-amplifiers developed to cope with 25ns colliding bunches
- Leakage current dealt with fast amplifiers
- Cost/unit area significantly reduced by growing larger diameter ingots (6" instead of 4"), single-sided processing (p-on-n)
- Implementation of front-end read-out chip in industry standard deep sub-micron technology

CMS Si-Tracker



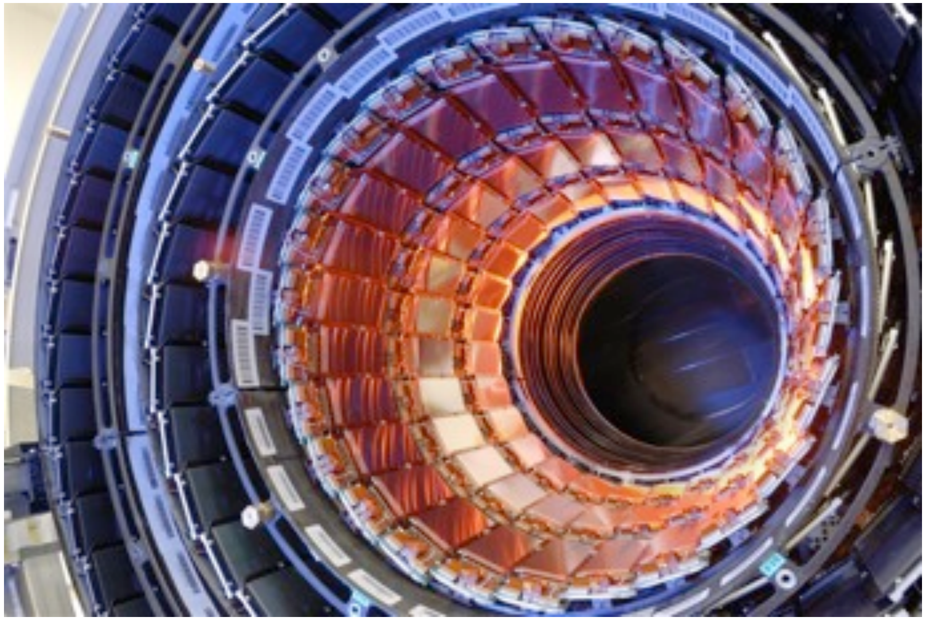
- Si-Strip-Detector:
  - ~ 210 m^2 Silicon
- 25 000 Sensors, 9.6 M channels
- 10 barrel layers, 2x 9 discs
- The largest ever built silicon tracker

CMS SI BARREL

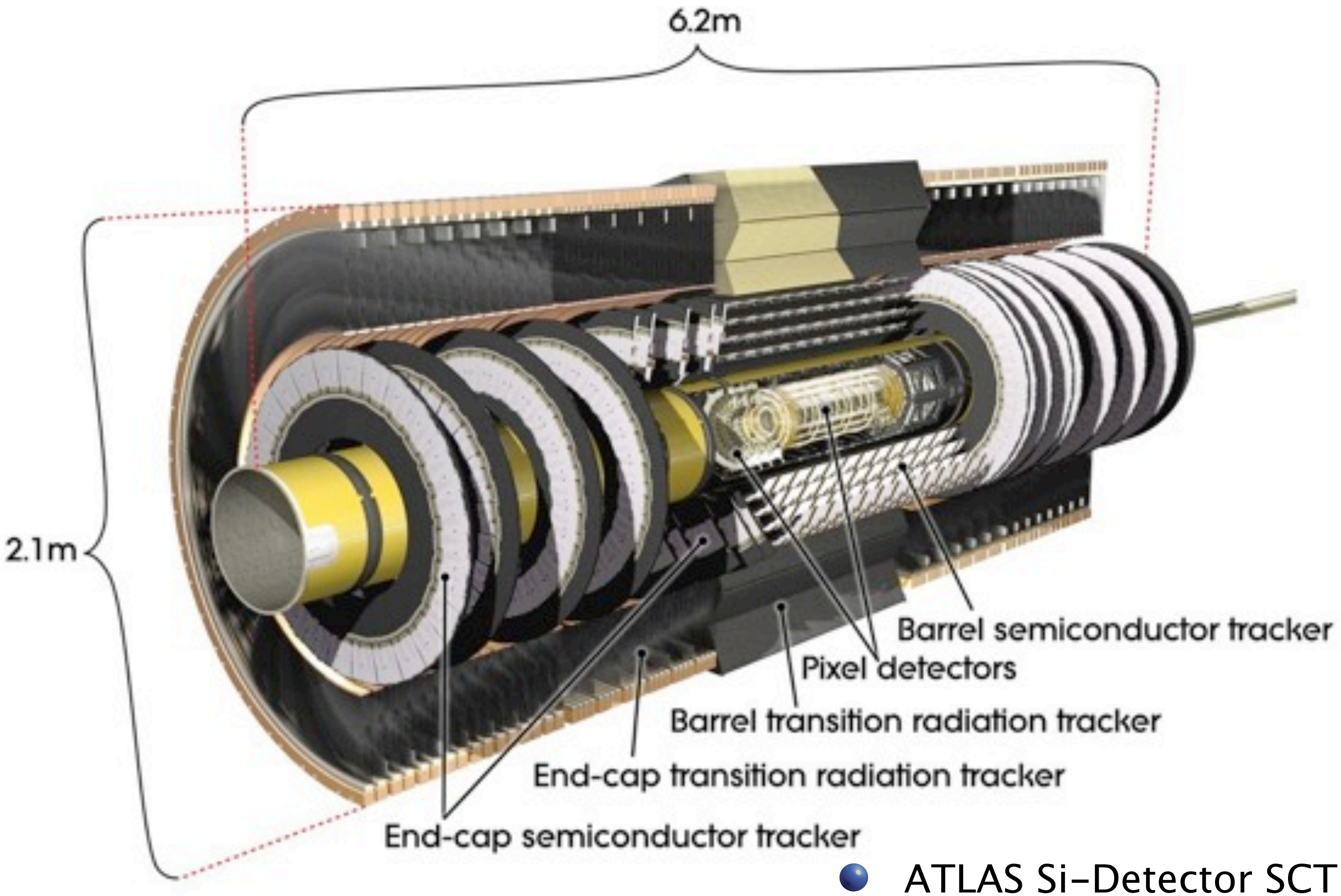


- Single and double sided layers

CMS Inner barrel Si Tracker: Single-Sided Si-Strip



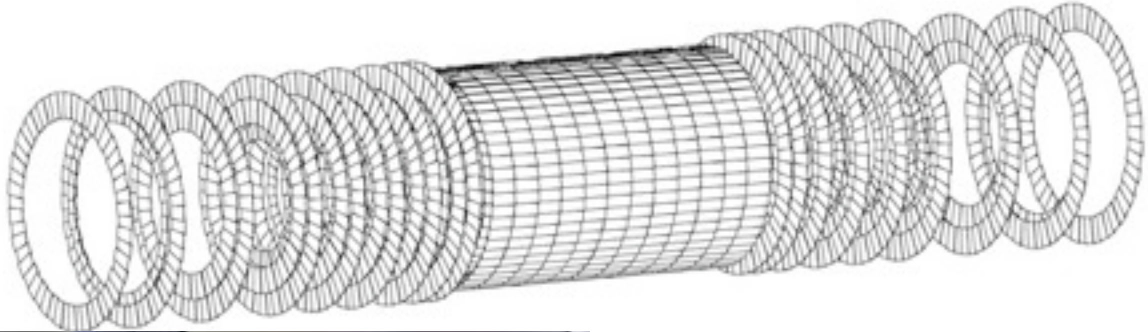
ATLAS SCT

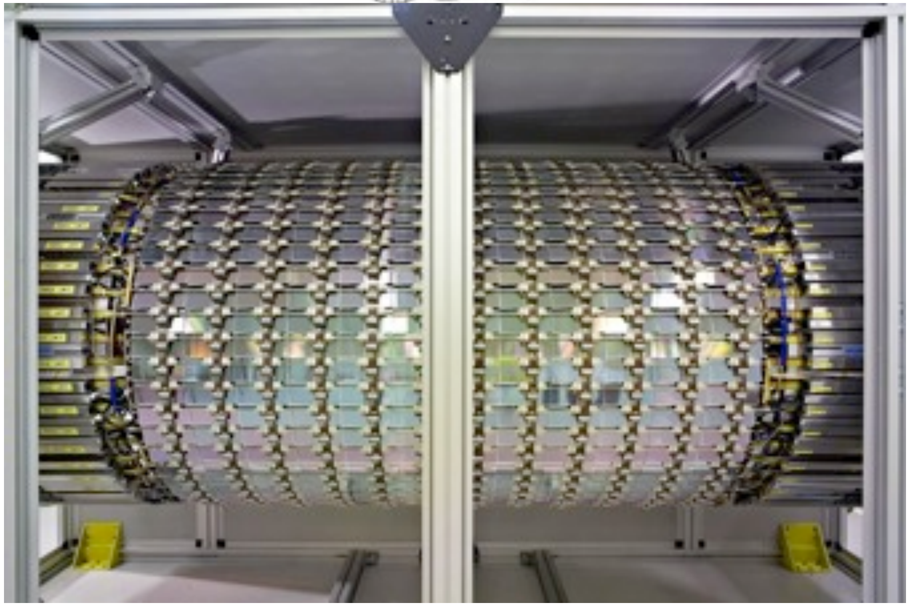


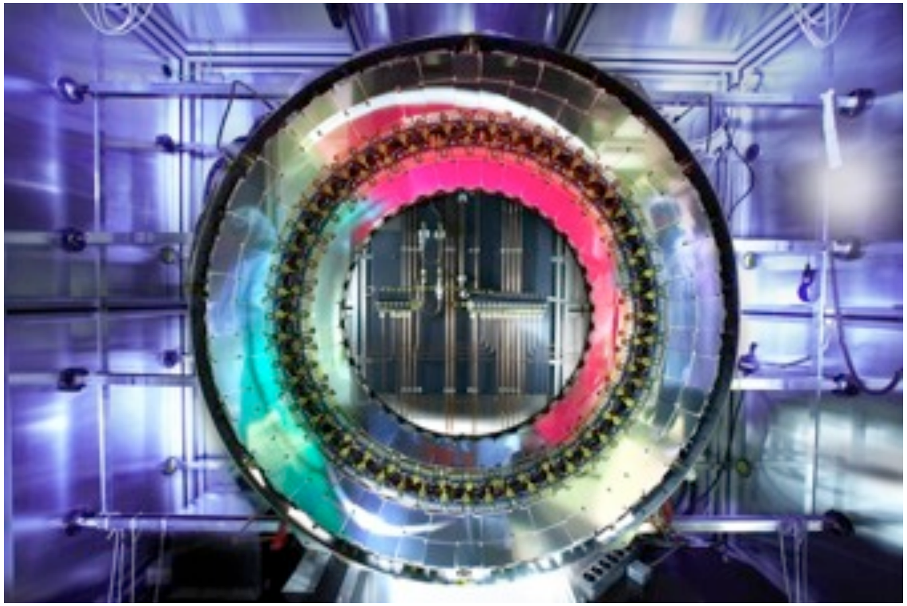
- ATLAS Si-Detector SCT:
  - Si- strips: 4 Barrel-layer, 2 x 9 discs

ATLAS SCT

- SCT strips:
  - 61 m^2 silicon, ~6.2 M channels
  - 4088 modules, 2112 barrel (1 type), 1976 in the discs (4 different types)

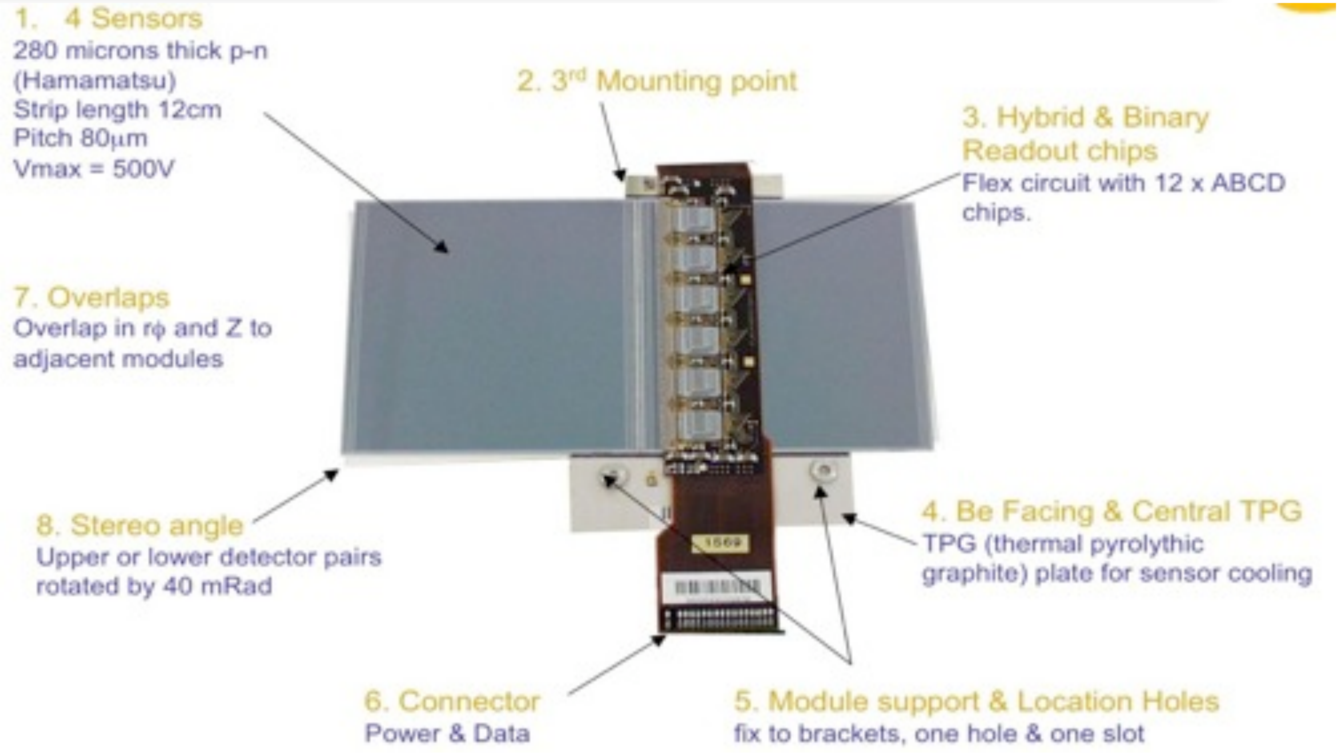






ATLAS SCT MODULE

barrel-module



1. 4 Sensors
280 microns thick p-n (Hamamatsu)
Strip length 12cm
Pitch 80μm
Vmax = 500V

2. 3rd Mounting point

3. Hybrid & Binary Readout chips
Flex circuit with 12 x ABCD chips.

4. Be Facing & Central TPG
TPG (thermal pyrolythic graphite) plate for sensor cooling

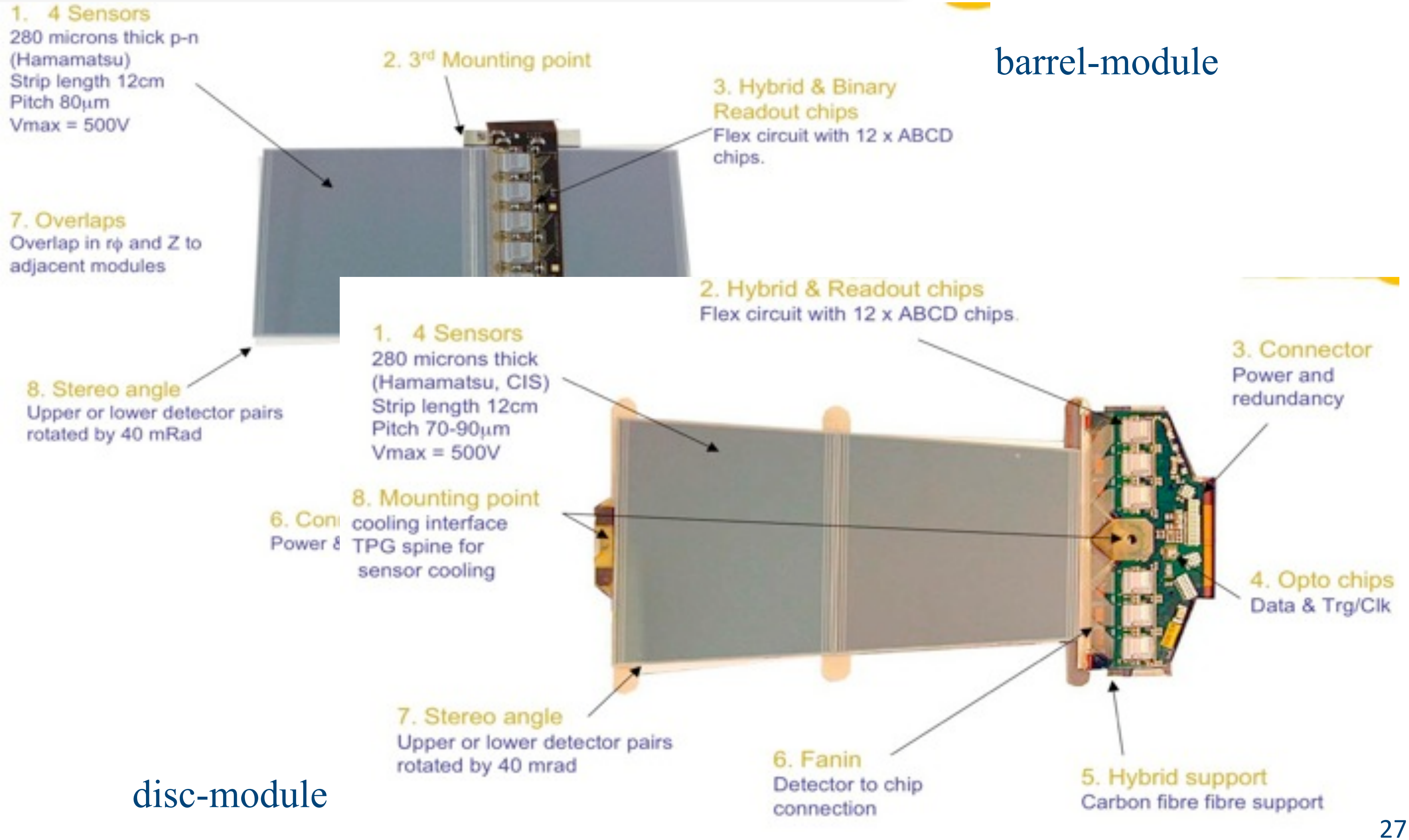
5. Module support & Location Holes
fix to brackets, one hole & one slot

6. Connector
Power & Data

7. Overlaps
Overlap in $r\phi$ and Z to adjacent modules

8. Stereo angle
Upper or lower detector pairs rotated by 40 mRad

ATLAS SCT MODULE



barrel-module

1. 4 Sensors
280 microns thick p-n (Hamamatsu)
Strip length 12cm
Pitch 80µm
Vmax = 500V

2. 3rd Mounting point

3. Hybrid & Binary Readout chips
Flex circuit with 12 x ABCD chips.

6. Con
Power &

7. Overlaps
Overlap in rφ and Z to adjacent modules

8. Stereo angle
Upper or lower detector pairs rotated by 40 mRad

disc-module

1. 4 Sensors
280 microns thick (Hamamatsu, CIS)
Strip length 12cm
Pitch 70-90µm
Vmax = 500V

2. Hybrid & Readout chips
Flex circuit with 12 x ABCD chips.

3. Connector
Power and redundancy

4. Opto chips
Data & Trg/Clk

5. Hybrid support
Carbon fibre fibre support

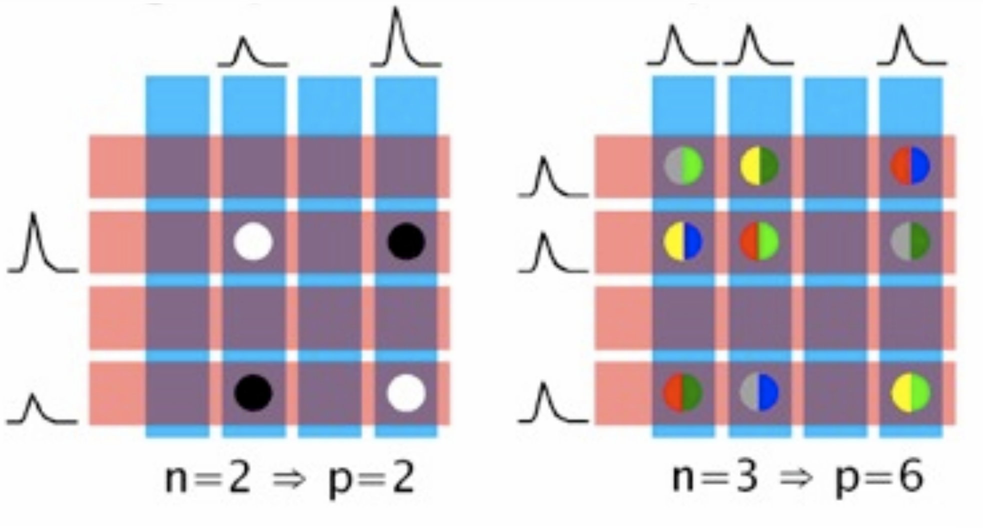
6. Fanin
Detector to chip connection

7. Stereo angle
Upper or lower detector pairs rotated by 40 mrad

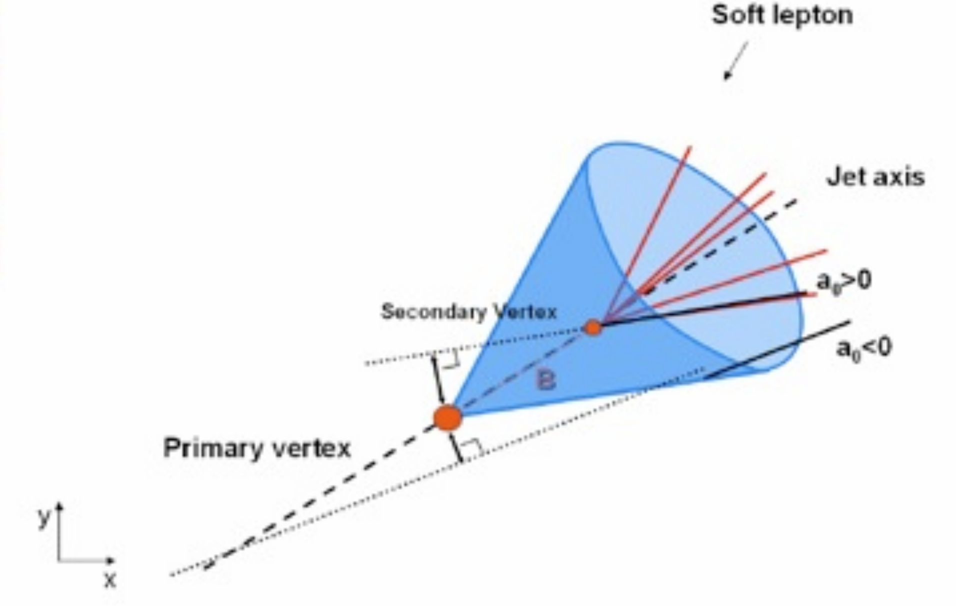
8. Mounting point
cooling interface
TPG spine for sensor cooling

PIXEL DETECTORS

LIMITS OF STRIP DETECTORS



- In case of high particle fluences ambiguities give difficulties for the track reconstruction



- Deriving the point resolution from just one coordinate is not enough information to reconstruct a secondary vertex
- Pixel detectors allow track reconstruction at high particle rate without ambiguities
- Good resolution with two coordinates (depending on pixel size and charge sharing between pixels)
  - Very high channel number: complex read-out
  - Readout in active area a detector

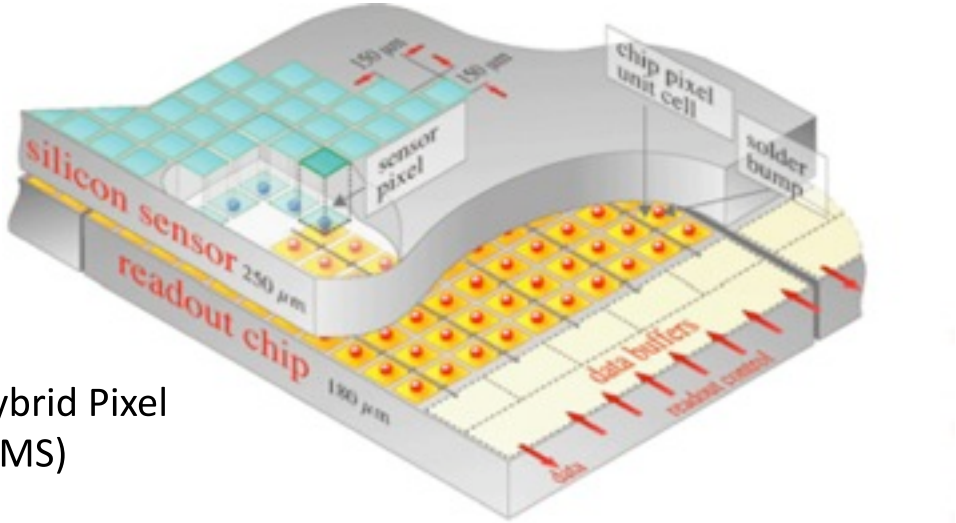
First pixels (CCDs)
in NA11/NA32: ~1983

HYBRID PIXELS – “CLASSICAL” CHOICE HEP

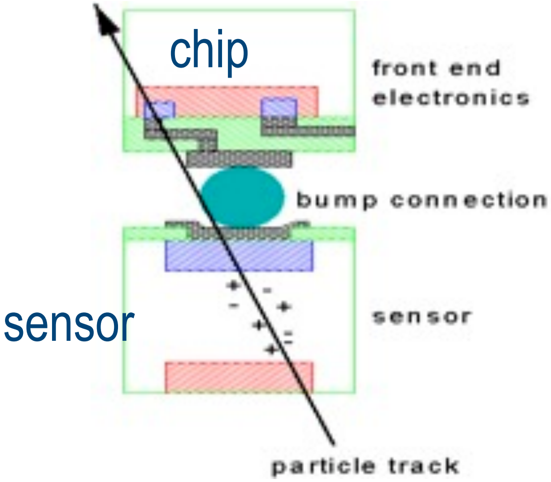
- The read-out chip is mounted directly on top of the pixels (bump-bonding)
- Each pixel has its own read-out amplifier
- Can choose proper process for sensor and read-out separately
- Fast read-out and radiation-tolerant

… but:

- Pixel area defined by the size of the read-out chip
- High material budget and high power dissipation

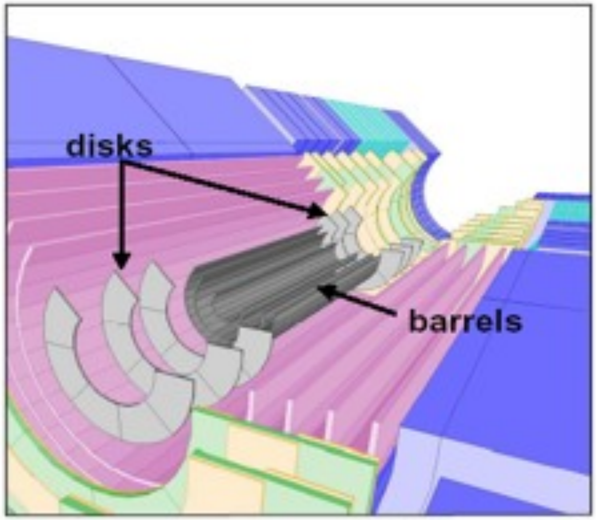


Hybrid Pixel
(CMS)



- CMS Pixels: ~65 M channels 150 µm x 150 µm
- ATLAS Pixels: ~80 M channels 50 µm x 400 µm (long in z or r)
- Alice: 50 µm x 425 µm
- LHCb
- Phenix upgrade
- Fair
- CBM
- PANDA

ATLAS-Pixels



A pixel module contains:

1 sensor (2x6cm)

~40000 pixels (50x500 mm)

16 front end (FE) chips

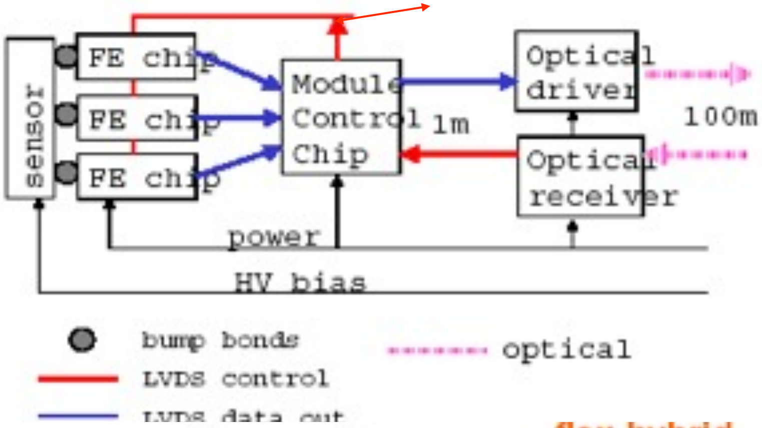
2x8 array

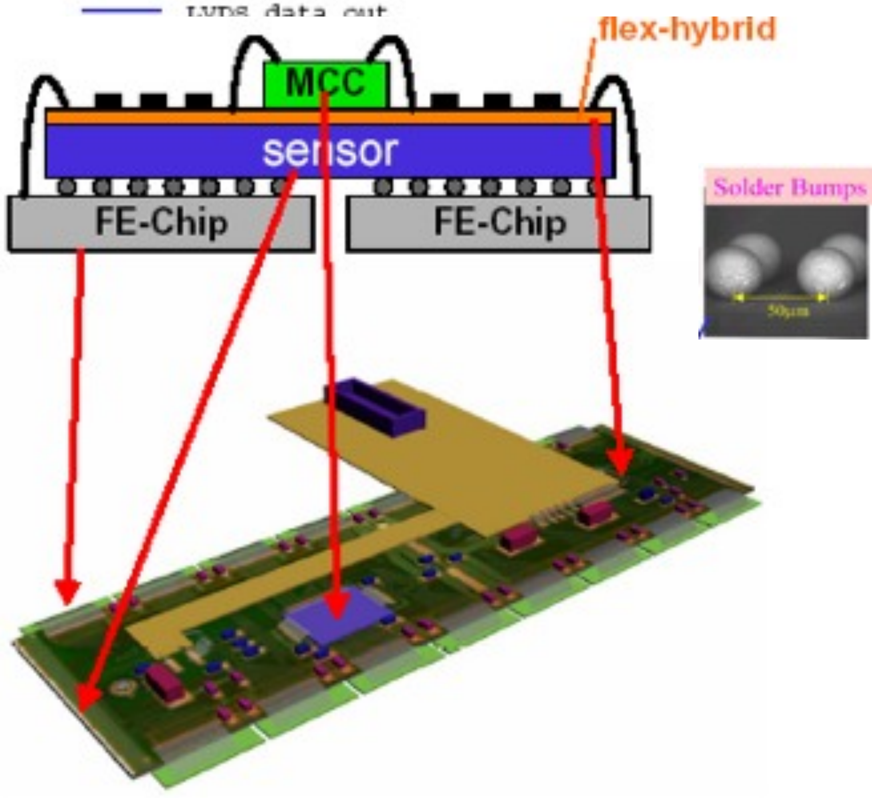
bump bonded to sensor

Flex-hybrid

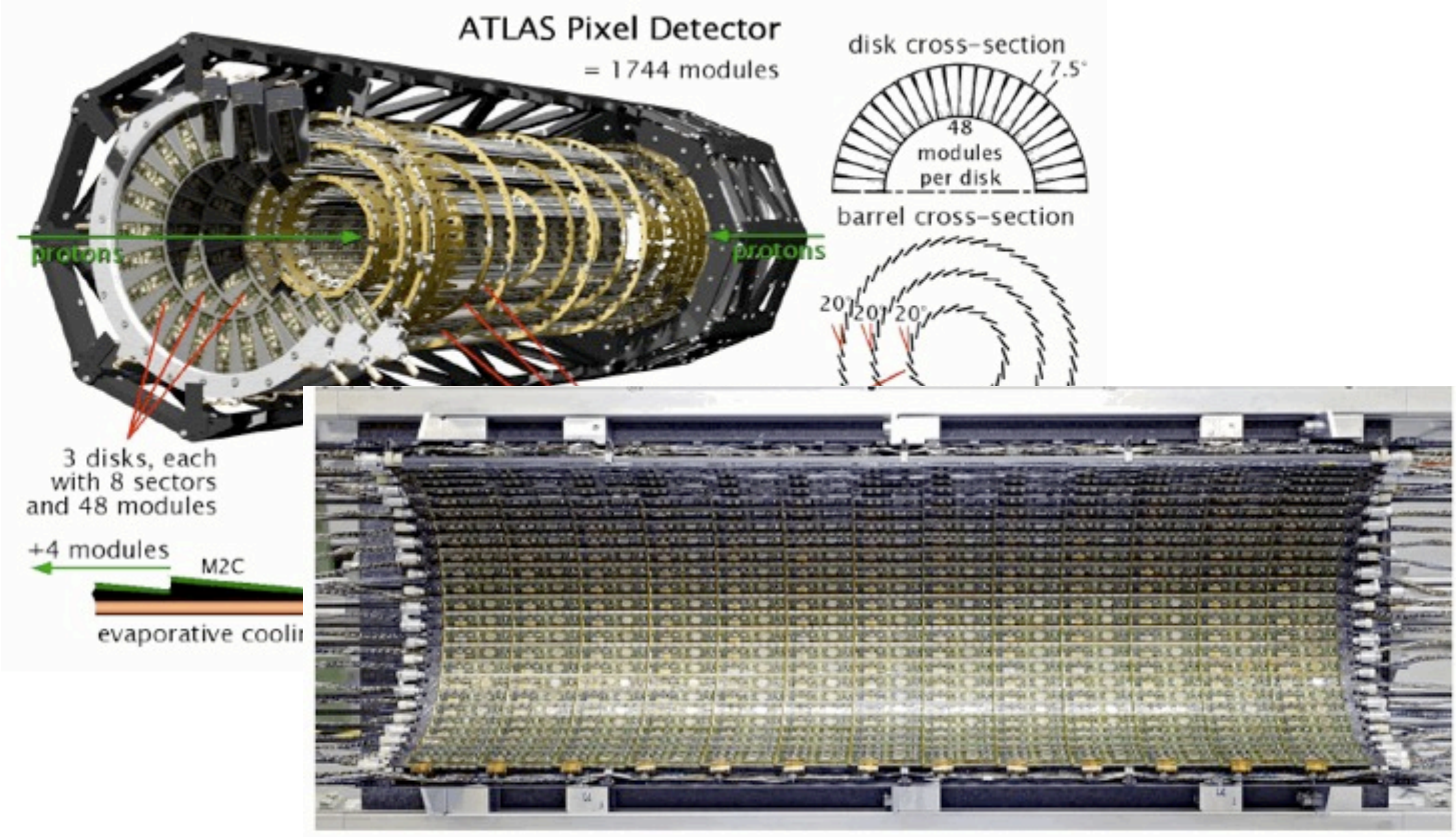
1 module control chip (MCC)

There are ~1700 modules

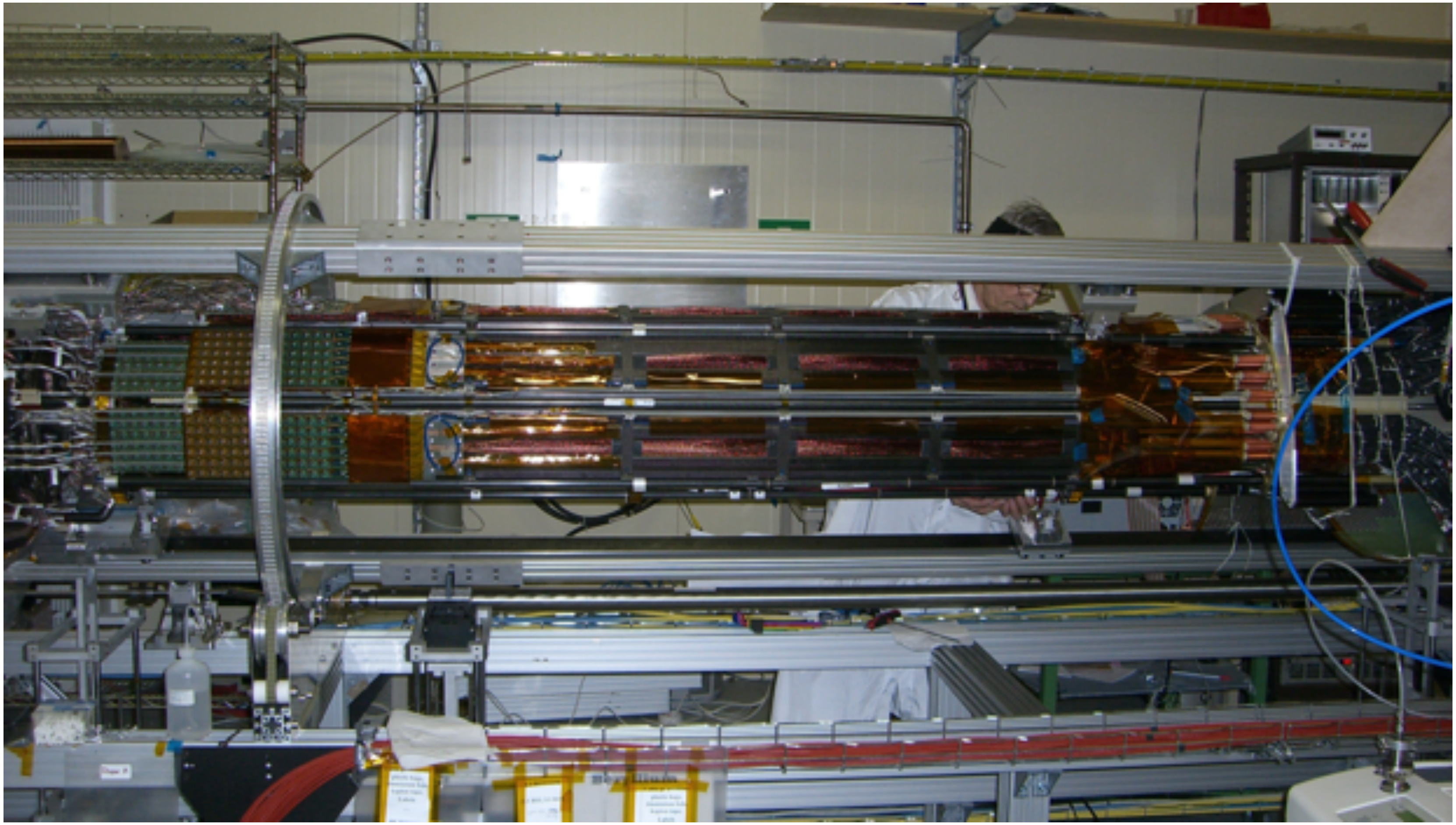




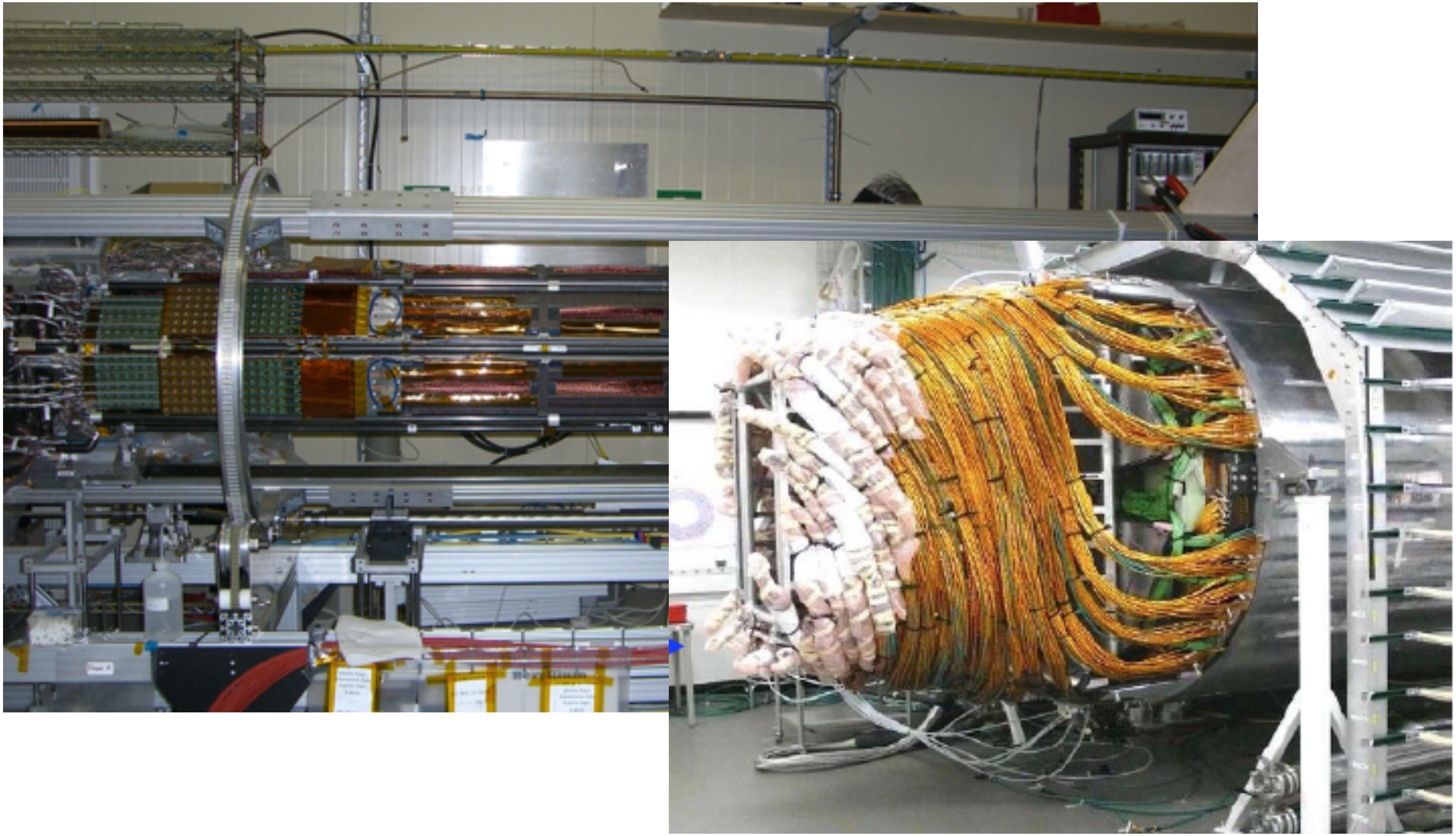
ATLAS-PIXELS



SERVICES!!

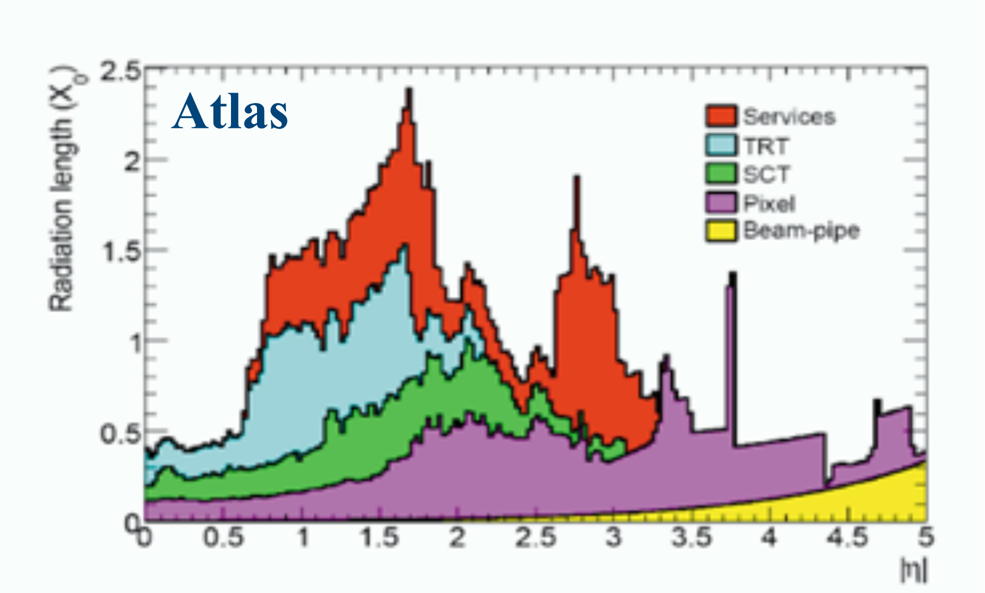


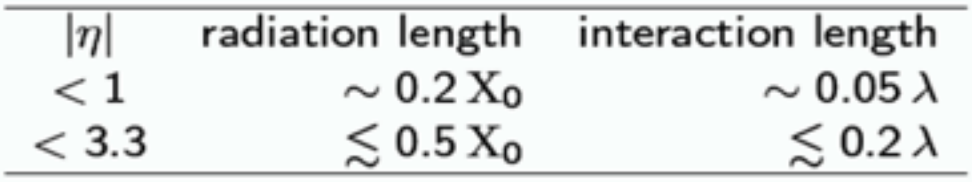
SERVICES!!



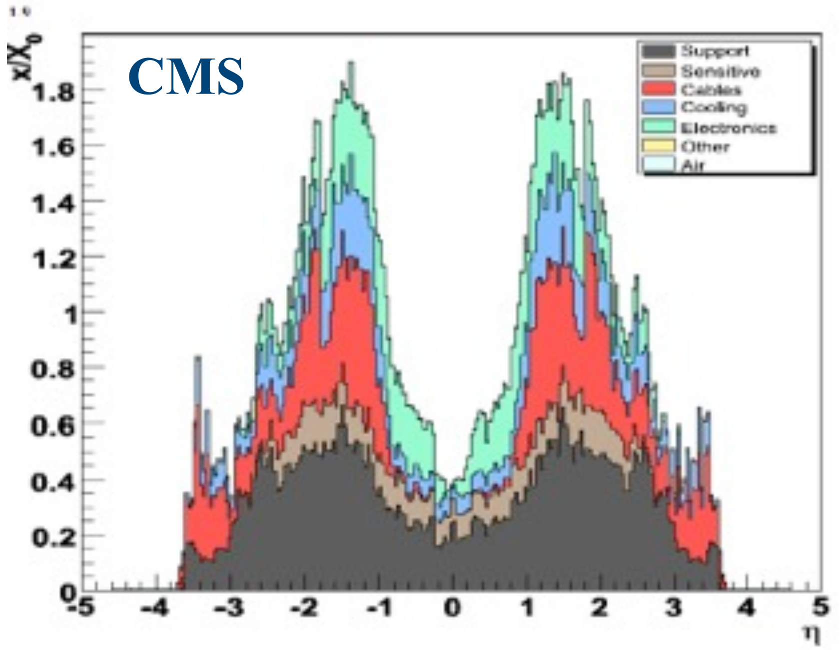
MATERIAL BUDGET OF LHC EXPERIMENTS

CMS & Atlas both slipped considerable in keeping X/X_0 originally aimed for !





$\vert\eta\vert$	radiation length	interaction length
< 1	$\sim 0.2\,X_0$	$\sim 0.05\,\lambda$
< 3.3	$\lesssim 0.5\,X_0$	$\lesssim 0.2\,\lambda$

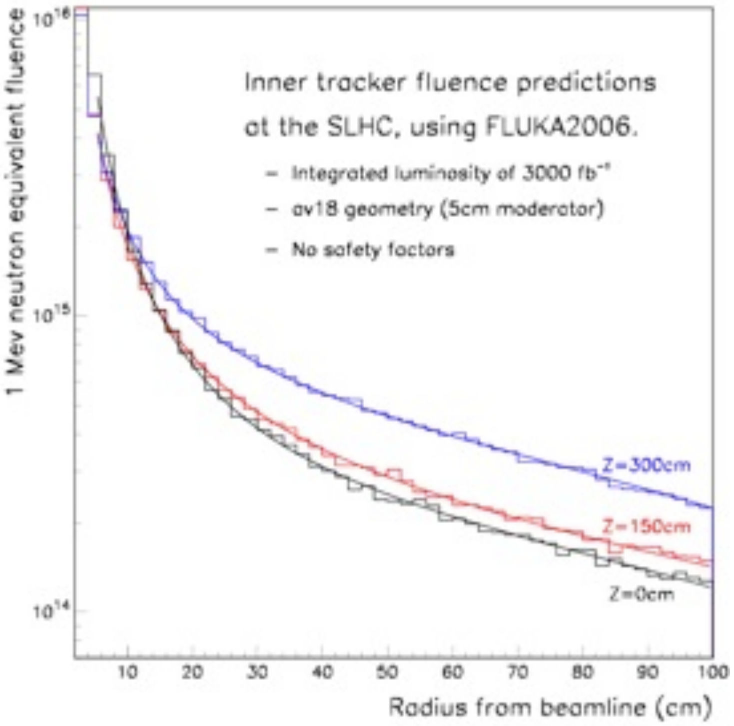


Old argument that Silicon would be too thick is not really true ==> **power & cooling**

NEXT GENERATION PIXEL DETECTORS

CURRENT CHALLENGES (ILC, sLHC)

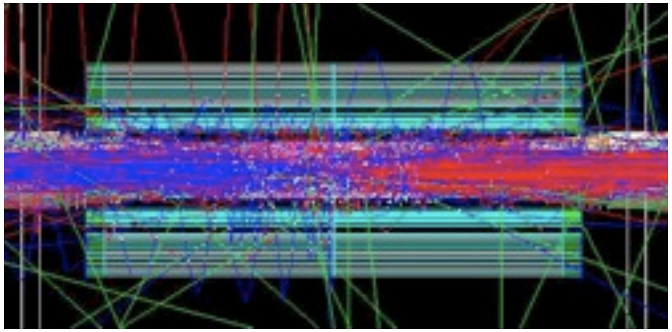
- Main challenge : identify c quark and $\tau^{\pm}$lepton jets
- life time ~10-12 sec => ~100um
- => particles decay within the vacuum beam pipe
- reconstruct decay products



Also here: Trend in tracking detectors: pixellised detectors installed very close to the beam interaction region

- Minimal distance limitations :
    - beam pipe radius
    - beam associated backgrounds
    - density of particles produced at the IP

- **Consequences on occupancy and radiation level**



OPTIMISING = COMPROMISING

- Conflict between physics performance driven parameters and running condition constraints :
  - Physics performance : spatial resolution and material budget (+ distance to IR)
  - Running conditions : read-out speed and radiation tolerance
  - Moreover :
    - ➡ limitations from maximum power dissipation compatible with running conditions and material budget
    - ➡ limitations from highest data flow acceptable by DAQ

- Ultimate performance on all specifications cannot be reached simultaneously
  - each facility & experiment requires dedicated optimization (hierarchy between physics requirements and running constraints
  - there is no single technology best suited to all applications
  - explore various technological options
  - motivation for continuous R&D (optimum is strongly time dependent)

PHYSICS OR RUNNING CONDITIONS

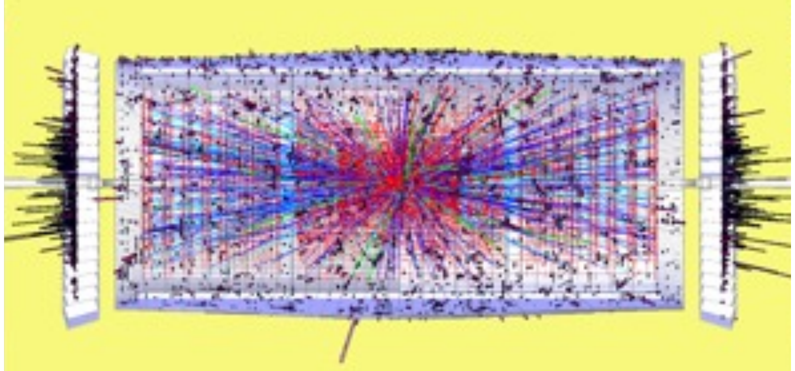
Physics performance driven :

- thin (potentially undepleted) sensitive volume
- ILC, RHIC, CLIC, SuperB, FAIR

➔ CMOS sensors, CCDs, DEPFETs, Vertically integrated (“3D”)

Running conditions driven :

- ”thick” depleted sensitive volume
- LHC & SLHC
- Hybrid pixel sensors, 3D sensors, Vertically integrated (“3D”)



Future : 3D integrated pixel devices

➔ reduce the gap between the two main optimization options

Two types of 3D:

3D sensors -> Cinzia DaVia

3D intergrated devices -> Christian Kiesling

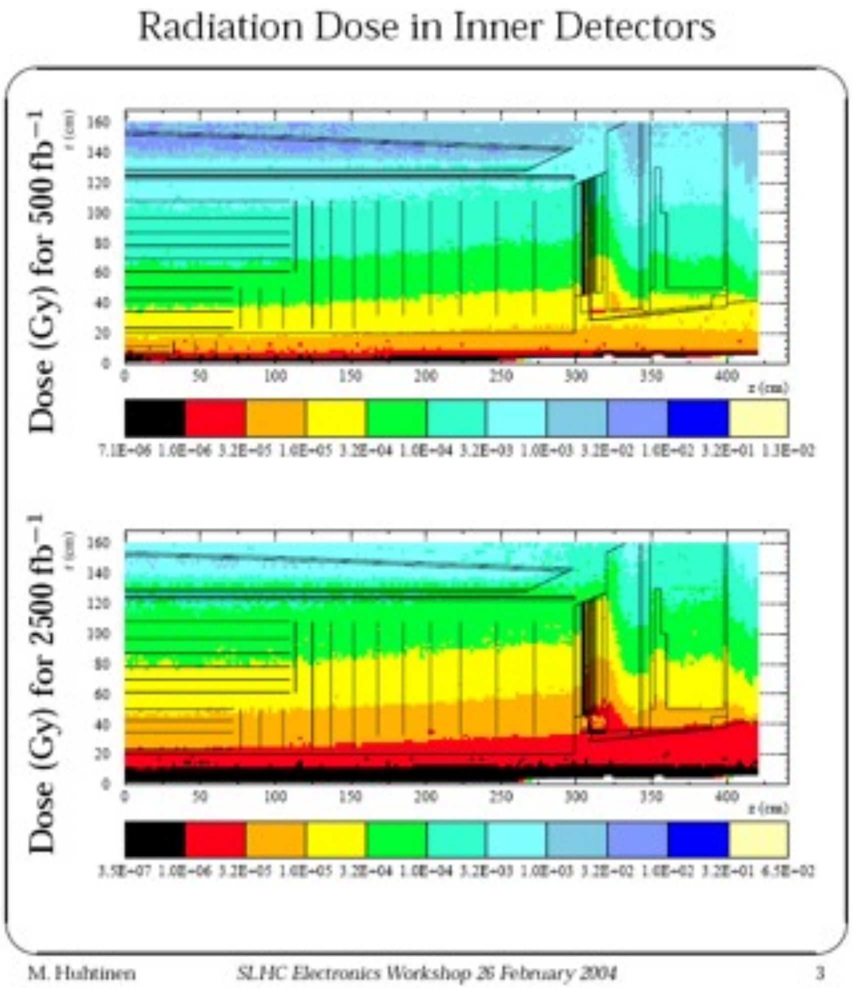
HARSH RUNNING CONDITIONS - SLHC

- 300 – 400 pile-up events at start of fill
- want to survive at least 3000 fb^{-1} data taking
- B-layer at 37 mm:
  - ~30 tracks per cm^{-2} per bunch crossing
  - > 10^{16} 1MEV n-equivalent non-ionising
  - Few 10s of MGray (10 x LHC)

- Improvement/evolution of hybrid pixel sensors :
  - Smaller CMOS feature size ➔ more compact FE µcircuits

    ➔ smaller pixels ➔ occupancy
  - Improved sensitive volume radiation hardness
  - Larger number of pixels ➔ power dissipation is an issue !

- Alternatives to hybrid pixels :
  - Particularly in fashion : 3D sensors
  - Others : 3D integrated devices



Radiation Dose in Inner Detectors

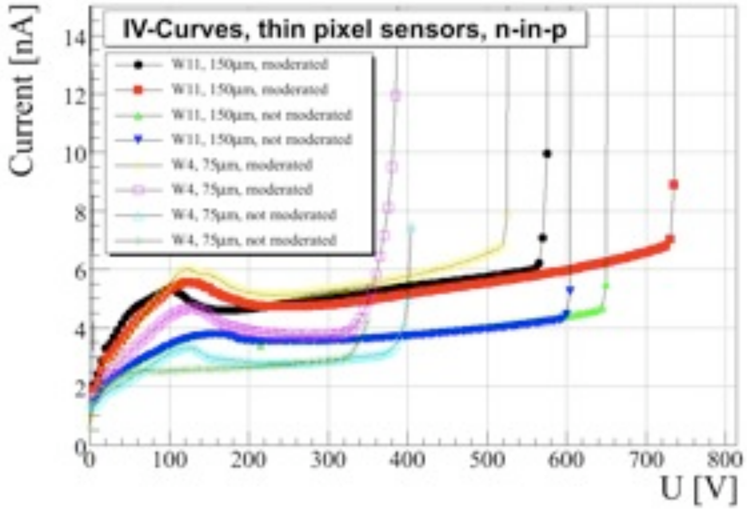
M. Huhtinen *SLHC Electronics Workshop 26 February 2004* 3

THIN PLANAR PIXEL SENSORS

1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process on top side
5. structure resist, etch backside up to oxide/implant

Thin planar pixels for the inner layers of the new ATLAS pixel system at SLHC:

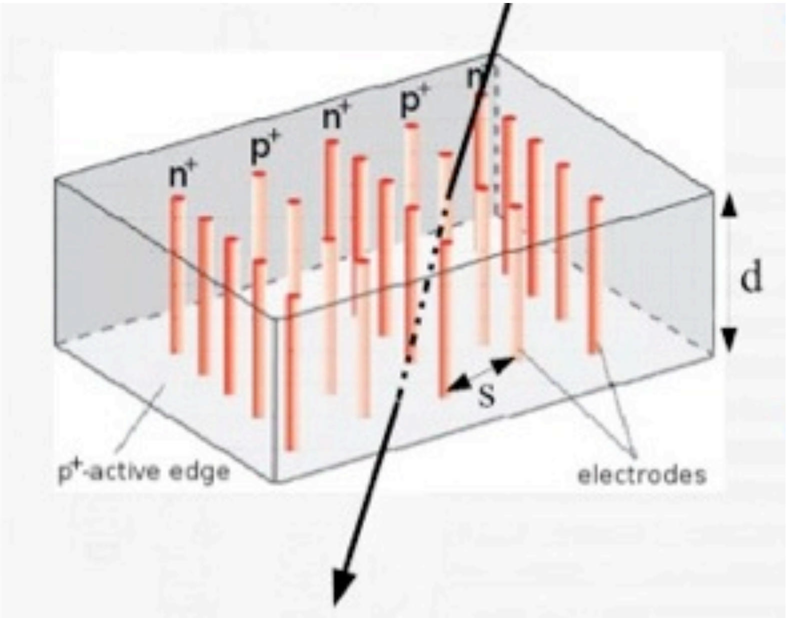
- At the same voltage thin (= over depleted) detectors are expected to have a higher electric field than thick (= partially depleted) detectors.
- They contribute to keep the material budget low, which is extremely important in the inner layers to maintain good tracking performances.

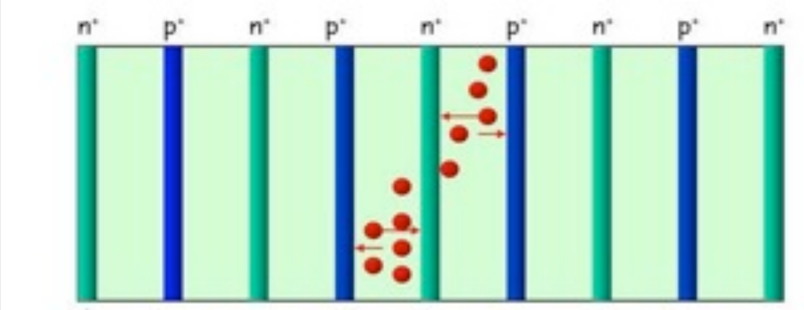


Results of a first characterization of the pixel structures on p-type wafers:

- Low leakage currents (<7 nA/cm^2 for 75 µm structures, <15 nA/cm^2 for 150 µm structures).
- Depletion voltages around 20 and 80 V for the 75 µm and 150 µm thick structures respectively
- High V_{break} for all the pixel structures produced

3D SENSORS





Both electrode types are processed inside the detector bulk instead of being implanted on the wafer's surface.

- 3-d array of p and n electrodes that penetrate into the detector bulk
- Lateral depletion:
  - Max. drift and depletion distance set by electrode spacing
  - Reduced collection time and depletion voltage
  - Thicker detectors possible
  - Low charge sharing

BUT: non-standard (planar) technology

THE VERTEX DETECTOR AT THE ILC

Measure impact parameter, charge for every charged track in jets, and vertex mass.

Need:

- Good angular coverage with many layers close to vertex:
  - $|\cos\theta| < 0.97$.
  - First measurement at r ~ 15-16 mm.
  - 5-6 layers out to r ~ 60 mm.
- Efficient detector for very good impact parameter resolution
- Material ~ 0.1% X_0 per layer.
- Capable to cope with the ILC beamstrahlungs background
- Modest average power consumption < 100W
- Single point resolution better than 3 µm.

- **small pixels, thin sensors, thin r/o electronics, low power (gas cooling)**

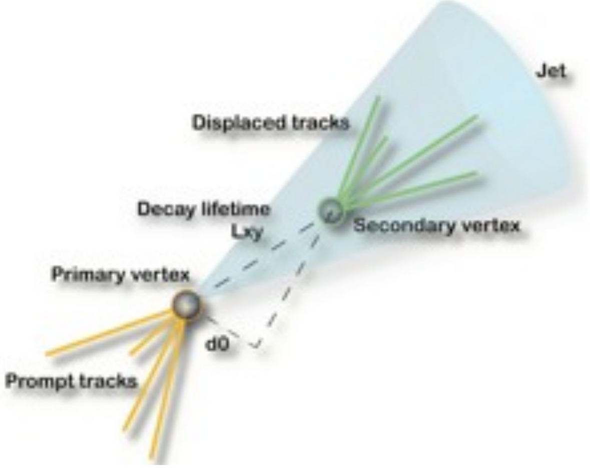


Figure of merit for the VXD:

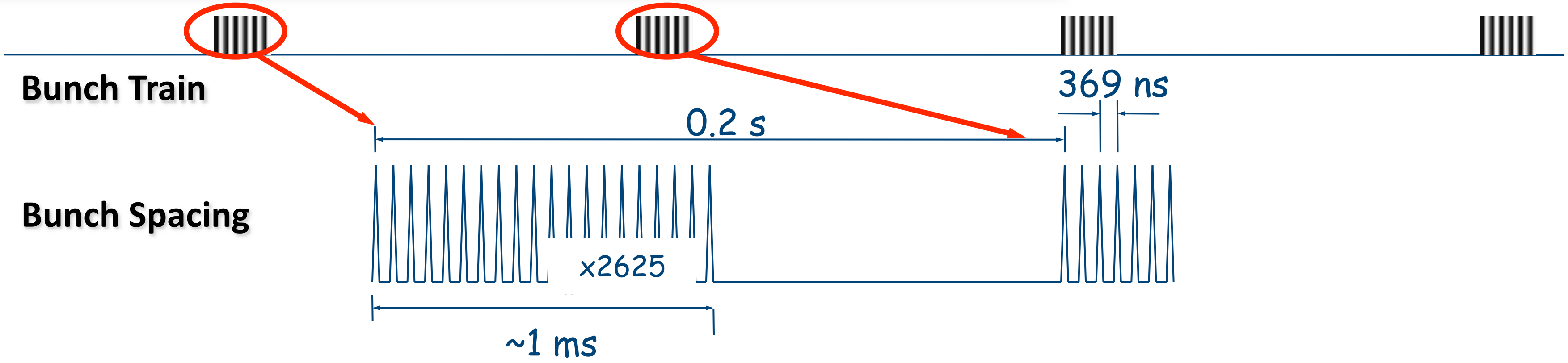
Impact Parameter Resolution

$$\sigma_{r\phi} \approx \sigma_{rz} \approx a \oplus b/(p\sin^{3/2}\vartheta)$$

Accelerator	a (µm)	b (µm)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC-II	13	19
ILC	**<5**	**<10**

(Marc Winter)

THE VERTEX DETECTOR AT THE ILC



- Inner layer 1.6 MPixel sensors
  - Once per bunch = 300ns per frame : too fast
  - Once per train ~100 hits/mm^2 : too slow
  - 5 hits/mm^2 => 50µs per frame: may be tolerable

    (Note: fastest commercial imaging ~ 1ms / MPixel)
- Four different technologies under study for ILC vertex detector
  - CCD, DEPFET, CMOS, and 3D
  - different variants of each technology approach under investigation
- The main split is between these 2 categories :
  - continuous read-out inside trains
  - delayed read-out in between consecutive trains

ILC: WHAT'S ON THE PIXEL MARKET?

- Currently there are about ~10 “candidates” for the ILC VTX Detector.
- These technologies have different approaches to cope with beam induced background at the ILC
- All approaches aim for ~3 μm precision and <40 mm 2-hit resolution
- Target material budget is ~0.1% X_0 per layer

single-bunch time stamping

"hybrid pixels w/o bumps"

- 3D integrated pixels (Fermilab)
- SOI (Fermilab, LBNL)
- ChronoPixels (Yale/Oregon)
- Deep N-Well MAPS SDR (INFN Milan, Pavia, RomaIII Uni. Bergamo, Insubria, Pavia)

Accumulation of ~70-150BX

1. cont. r/o during train

- CPCCD (LCFI)
- DEPFET
- Mimosa (Strasbourg at al.)

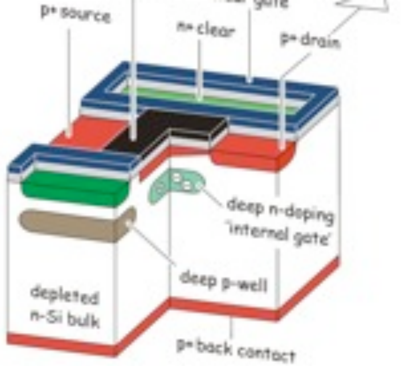
2. store and r/o in pause

- CAPs (Hawaii)
- ISIS (LCFI)

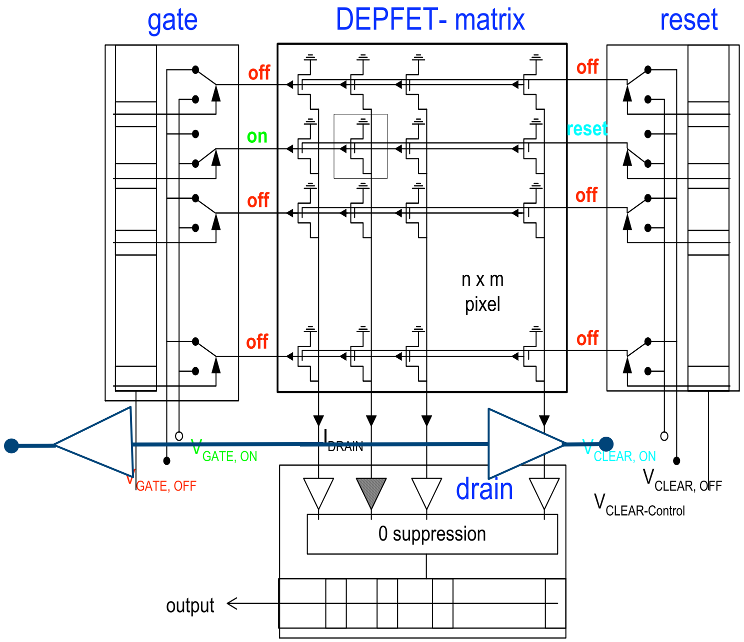
Accumulation of about 3000BX

- FP-CCD (KEK, JAXA/ISAS, Tohoku Uni)

DEPFET



- DePletedFeld Effect Transistor

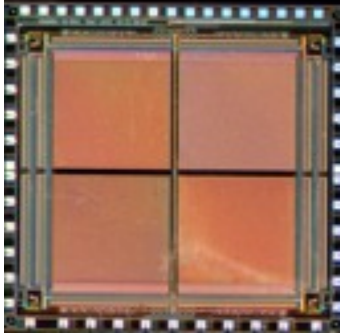


- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster size
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- internal amplification
  - large signal, even for thin devices
  - r/o cap. independent of sensor thickness
  - charge-to-current conversion: $g_q = dI_d/dq \approx 1$ nA/electron, scales with gate length
- Charge collection in "off" state, read out on demand

- Row wise read-out ("rolling shutter"): select row with external gate, read current, clear DEPFET, read current again → the difference is the signal
- only one row active → low power consumption
- But: for 40kHz frame rate → 25ns per row l

DEPFET is baseline technology
for the vertex detector of SuperBelle

MONOLITHIC ACTIVE PIXELS (MAPS)

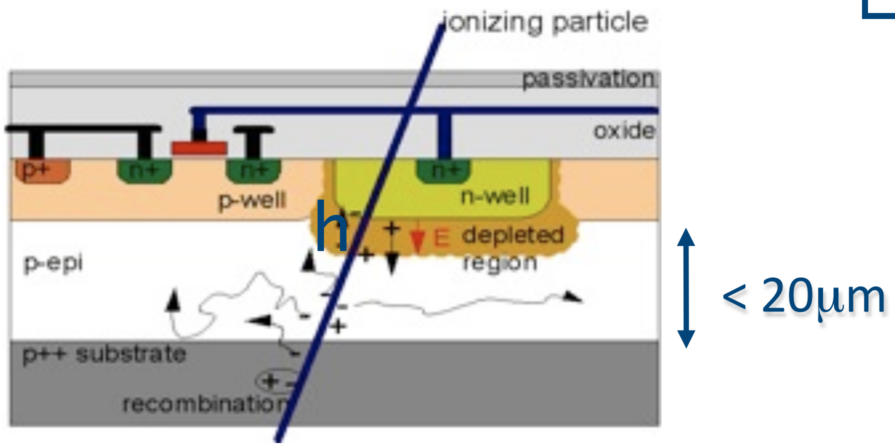


- e.g. Mimosa (Minimum Ionizing Particle MOS Active Pixel Sensor)

- Active area underneath the electronics (epi-layer <20µm thick) providing 100% fill-factor
- Charge generated by ionization in the epitaxial layer thermally diffuse toward low potential n-well region
- Standard, cost-effective CMOS process, no post-processing

Features of the MIMOSA – detectors:

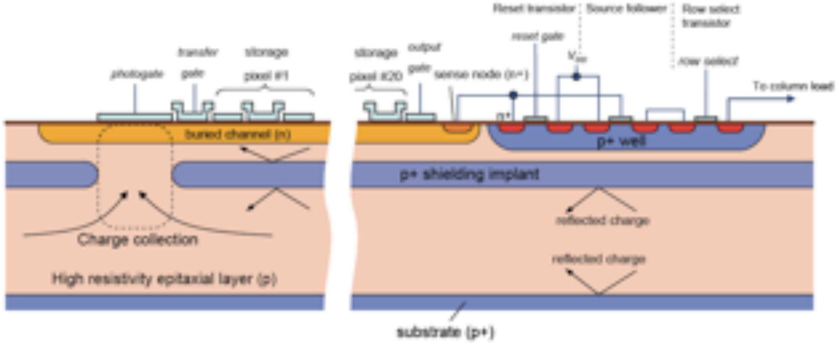
- Single point resolution 1 µm – 3 µm
- Pixel – pitch 10-40 µm
- Thinning achieved 50 - 120µm
- S/N for MIPs 20 – 40
- Detection efficiency > 99%
- Radiation hardness: 1MRad ; 2 x 10^{13} n_{eq}/cm^2
- Produced in various commercial CMOS-processes



Mimosa is baseline technology for the vertex detector of STAR

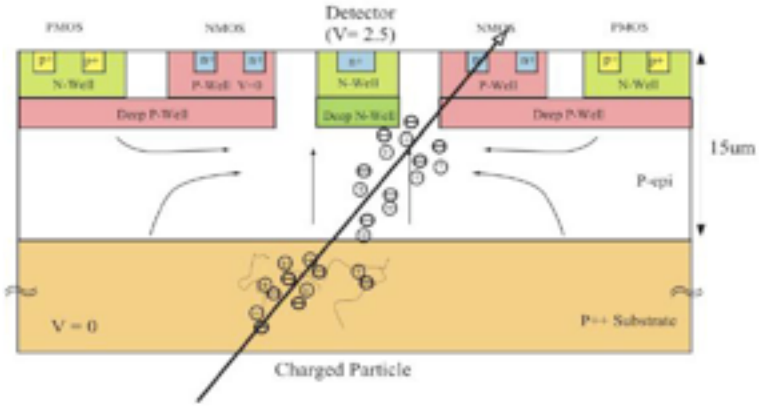
CCD BASED

- Charge-Coupled Devices (CCDs)
  - Demonstrated in large system (307Mpx) at SLD, but slow.
- Column Parallel CCDs (CPCCD)
  - column parallel readout, with bump-bond connections on 20 μm pitch to readout chip including amp, analogue CDS, ADCs, sparsification and memory
- FPCCD (Fine Pixel CCD) – fully depleted epi-layer to suppress diffusion
  - with 5 μm pixels, read out once per train; 20 times finer pixel granularity instead of 20 time slices

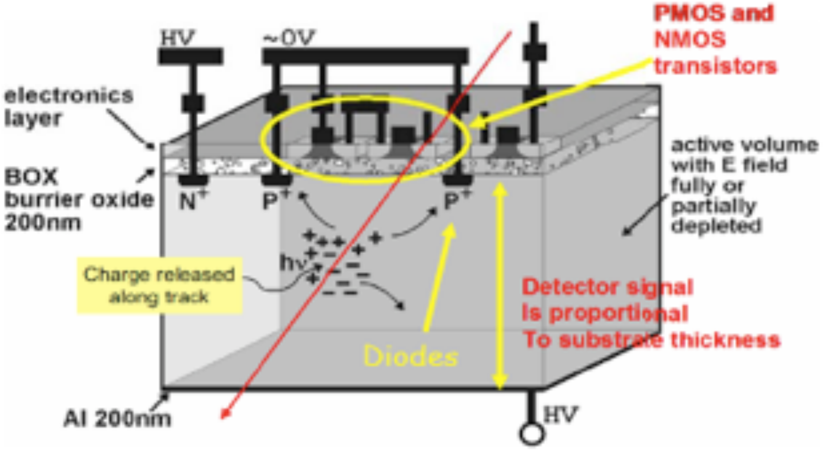


- Image Sensor with In-Situ Storage (ISIS)
  - Combines CCDs, active pixel transistors and edge electronics in one device
  - Charge collected under a photo-gate
  - Charge is transferred to 20-pixel storage CCD in situ, 20 times during the ~ 1 ms long bunch train

CHRONOPIXEL AND SOI

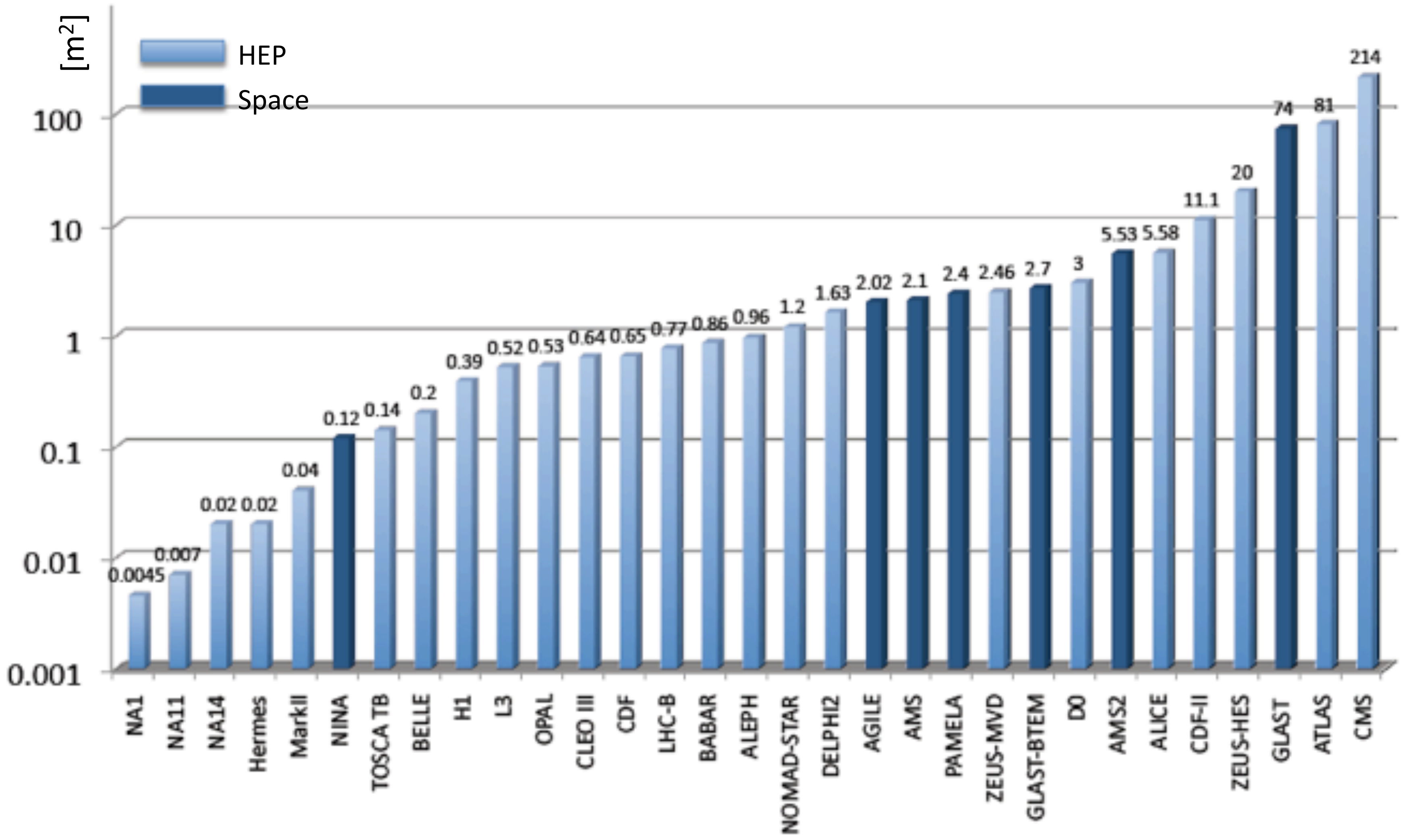


- Double CMOS Pixel
  - Macro (50 µm pitch) for timing
  - Micro (5 µm pitch) for precise position
  - Buffer data during ~3000 bunches in a train and readout between bunch trains



- SOI detectors are a first step toward 3D integration since it uses many of the same processes as 3D integration (oxide bonding, wafer thinning, via formation)
  - Thin top layer with silicon islands in which PMOS and NMOS transistors are built.
  - A buried oxide layer (BOX) which separates the top layer from the substrate.
  - High resistivity substrate which forms the detector volume.
  - Diode implants are formed beneath the BOX and connected by vias.

SILICON DETECTOR SIZE 1981 - 2006



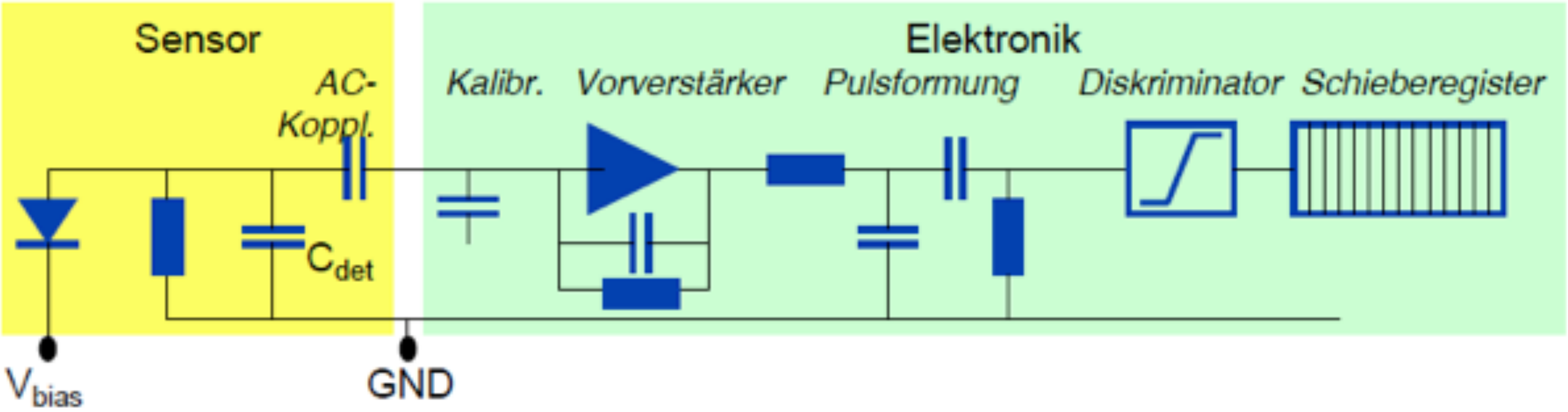
SUMMARY

Solid state detectors play a central role in modern high energy and photon physics

- Used in tracking detectors for position and momentum measurements of charged particles and for reconstruction of vertices (specially pixel detectors)
- By far the most important semiconductor: Silicon, indirect band gap 1.1 eV, however: 3.6 eV necessary to form eh pair
- Advantages Si: large yield in generated charge carriers, fine segmentation, radiation tolerant, mechanically stable, …
- Working principle (general) diode in reverse bias (pn junction)
- Important: S/N has to be good. Noise ~1/C for systems that measure signal charge smaller feature sizes are good. Pixel!

- Pixel detectors are used in most major current particle detectors and are planned for future experiment
- R&D for semiconductor detectors always has to be on the edge of technology

NOISE SOURCES



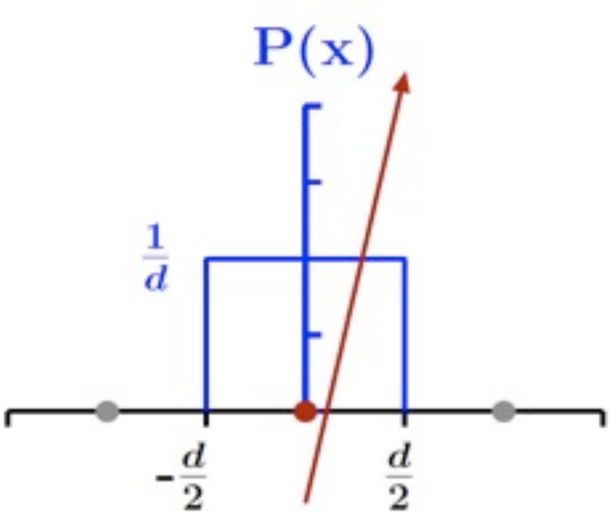
NOISE

- detector capacity $N_C \sim a + b \cdot C_{\text{det}}$ $(\sim \frac{1}{\sqrt{\tau}})$
- dark current $N_I \sim \sqrt{I \cdot \tau}$
- serial resistor $N_R \sim C_{\text{det}} \sqrt{\frac{R}{\tau}}$
- Segmentation into many channels $N_{\text{segment}} \approx \frac{N_{\text{all}}}{\sqrt{n}}$

RESOLUTION OF TRACKING DETECTORS

- Depending on detector geometry and charge collection
  - Strip pitch
  - Charge sharing between strips

Simple case: all charge is collected in one strip



- Simple case: all charge is collected by one strip
- Traversing particle creates signal in hit strip
- Flat distribution along strip pitch; no area is pronounced

➔ Probability distribution for particle passage:

$$P(x) = \frac{1}{d} \qquad \Rightarrow \int_{-d/2}^{d/2} P(x)\,dx = 1$$

The reconstructed point is always the middle of the strip:

$$\langle x \rangle = \int_{-d/2}^{d/2} x\,P(x)\,dx = 0$$

RESOLUTION OF TRACKING DETECTORS II

- Calculating the resolution orthogonal to the strip:

$$\sigma_x^2 = \langle (x - \langle x \rangle)^2 \rangle = \int_{-d/2}^{d/2} x^2 \, P(x) \, dx = \frac{d^2}{12}$$

- Resulting in a general term (also valid for wire chambers):

$$\sigma = \frac{d}{\sqrt{12}}$$

- For a silicon strip detector with a strip pitch of 80 μm this results in a minimal resolution of ~23μm
- In case of charge sharing between the strip (signal size decreasing with distance to hit position)
  - Resolution improved by center of gravity calculation

INTERACTIONS OF PARTICLES WITH MATTER

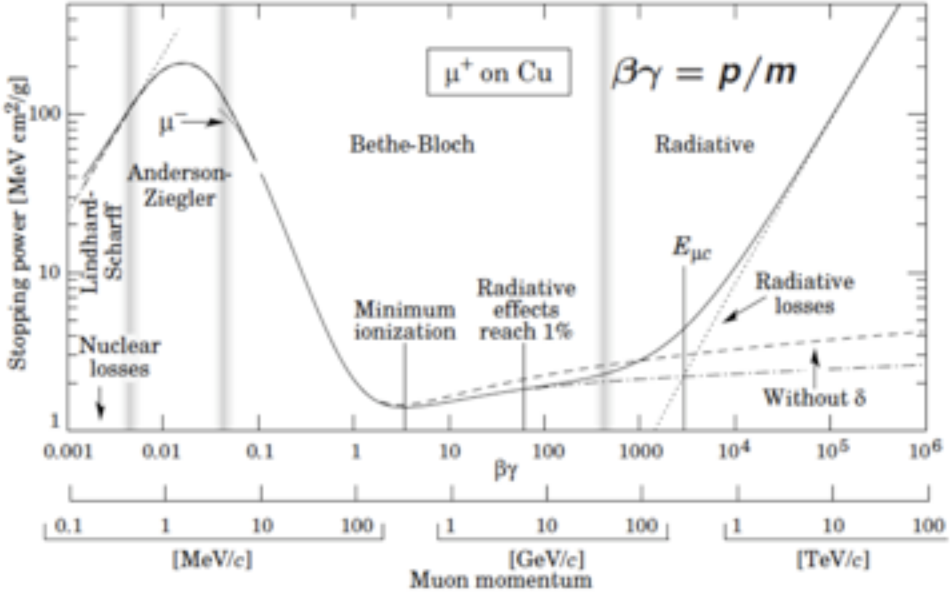
$$-\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A} \cdot \frac{1}{\beta^2} \cdot [\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2} - \beta^2 - \frac{\delta}{2} - \frac{C}{Z}]$$

$T_{\max}$ Maximum kinetic energy which can be transferred to the electron in a single collision

$\frac{\delta}{2}$ Density term due to polarization: leads to saturation at higher energies

I^2 Excitation energy

$\frac{C}{Z}$ Shell correction term, only relevant at lower energies



INTERACTIONS OF PARTICLES WITH MATTER

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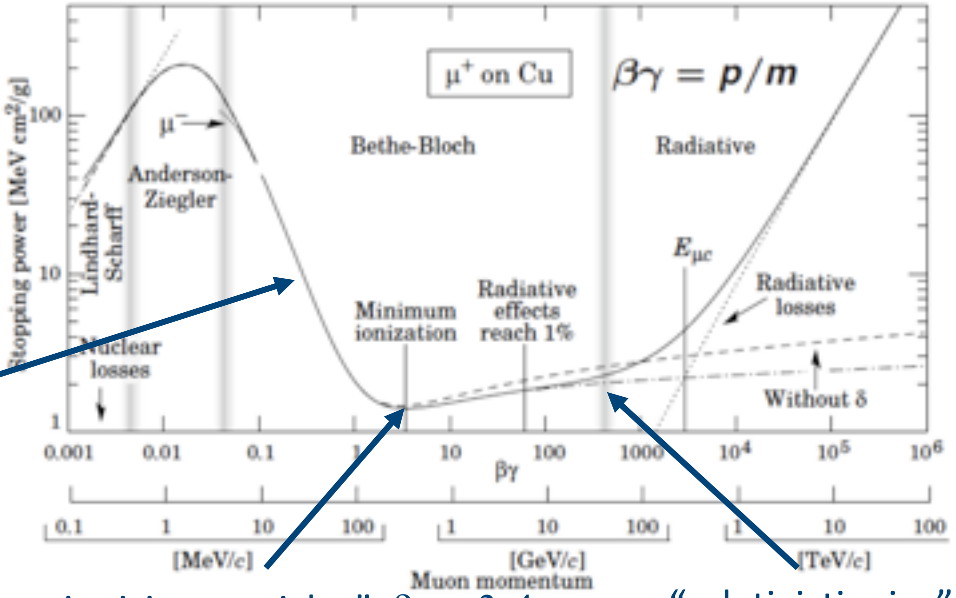


$$\left\langle \frac{dE}{dx} \right\rangle \propto \frac{1}{\beta^2}$$

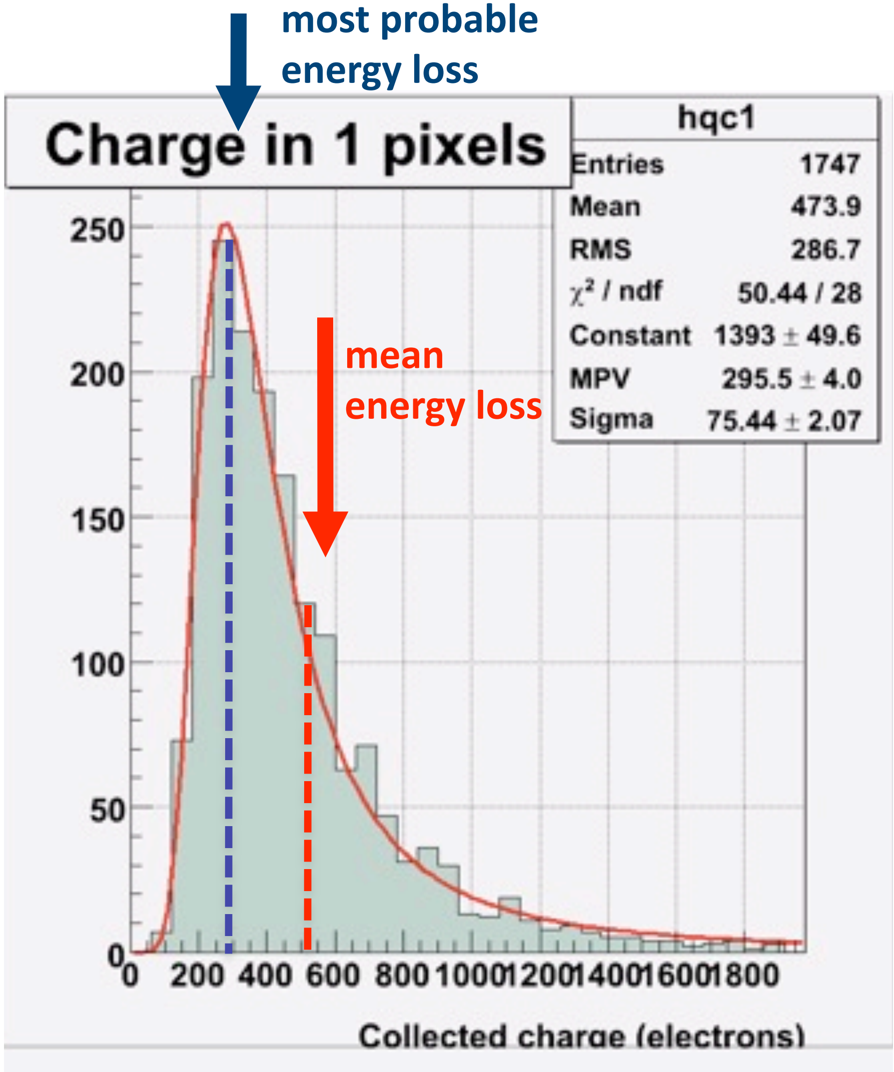
"kinematic term"

"minimum ionizing particles" $\beta\gamma \approx$ 3-4

"relativistic rise" $$\left\langle \frac{dE}{dx} \right\rangle \propto \ln \beta^2 \gamma^2$$

LANDAU DISTRIBUTION SILICON

- Bethe-Bloch describes average energy loss
- Collisions stochastic nature, hence energy loss is distribution instead of number.
- First calculated for thin layers was Landau. Hence energy loss is Landau distributed.
- Signal proportional to energy loss



most probable energy loss

mean energy loss

Example:
Monolithic active pixel sensor
sensitive layer 14um

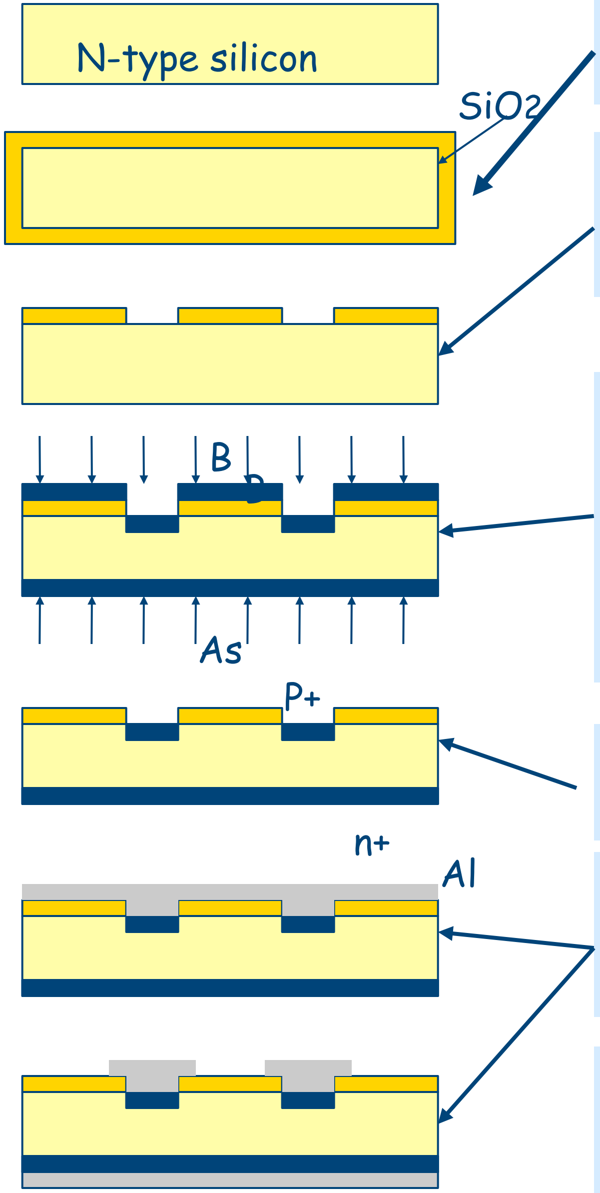
LITERATURE

- **Semiconductor Detector Systems**,
  Helmuth Spieler, Oxford University Press 2005

- **Pixel Detectors – From Fundamentals to Applications**
  L. Rossi, P. Fischer, T. Rohde, N. Wermes, Springer Verlag 2006

- **Evolution of Silicon Sensor Technology in Particle Physics**
  Frank Hartmann, Springer Verlag 2009

Planar process



n-type wafers are oxidized at 1030^{o}C to have the whole surface passivated.

Using photolithographic and etching techniques, windows are created in the oxide to enable ion implantation. Different geometries of pads and strips can be achieved using appropriate masks.

The next step is the doping of silicon by ion implantation. Dopant ions are produced from a gaseous source by ionisation using high voltage.The ions are accelerated in an alectric field to energy in the range of 10 keV-100 keV and then the ion beam is directed to the wondows in the oxide. P+ strips are implanted with boron, while phosphorous or arsenic are used for the n+ contacts.

An annealing process at 600^{o}C allows partial recovery of the lattice from the damage caused by irradiation.

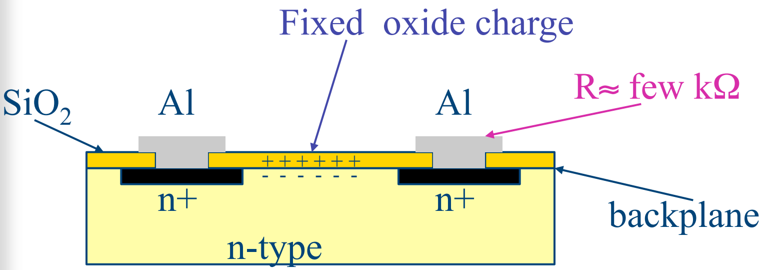
The next step is the metallisation with aluminium, required to make electrical contact to the silicon. The desired pattern can be achieved using appropriate masks.

The last step before cutting is the passivation, which helps to maintain low leakage currents and protects the junction region from mechanical and ambient degradation.

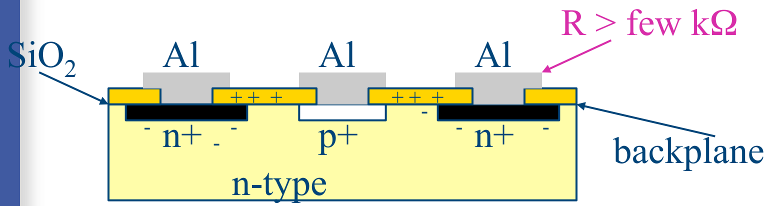
DOUBLE-SIDED STRIP DETECTORS

Since the micro-strip detector provides only one coordinate with good precision, the segmentation of the backplane is a natural way to provide a second coordinate and thus a space point without adding material on the trajectory of the particles.

The use of double-sided micro-strip detectors allows the correlation of signals collected on the two sides, which apart from the readout electronics noise and response is the same, thus reducing multi-hit ambiguities.

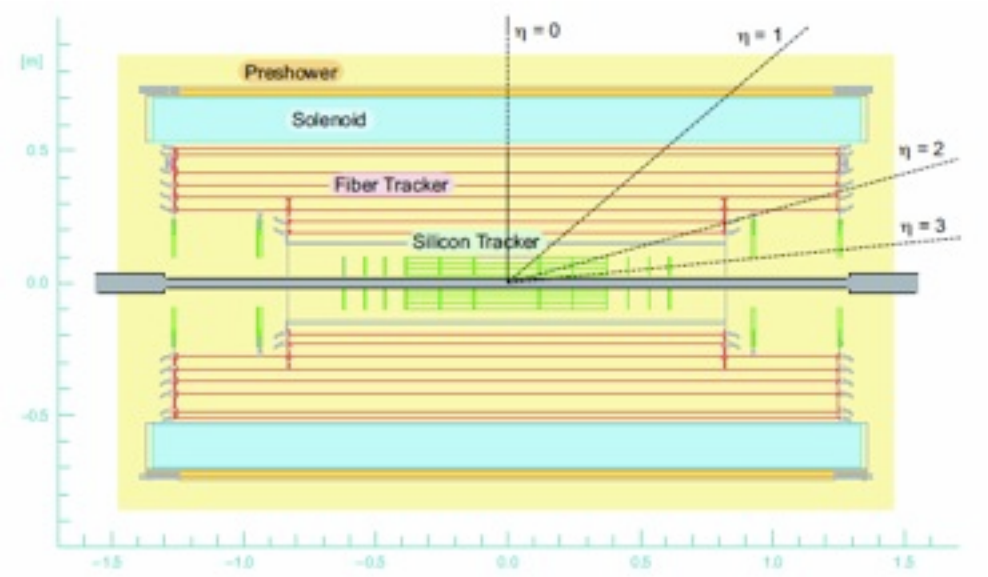


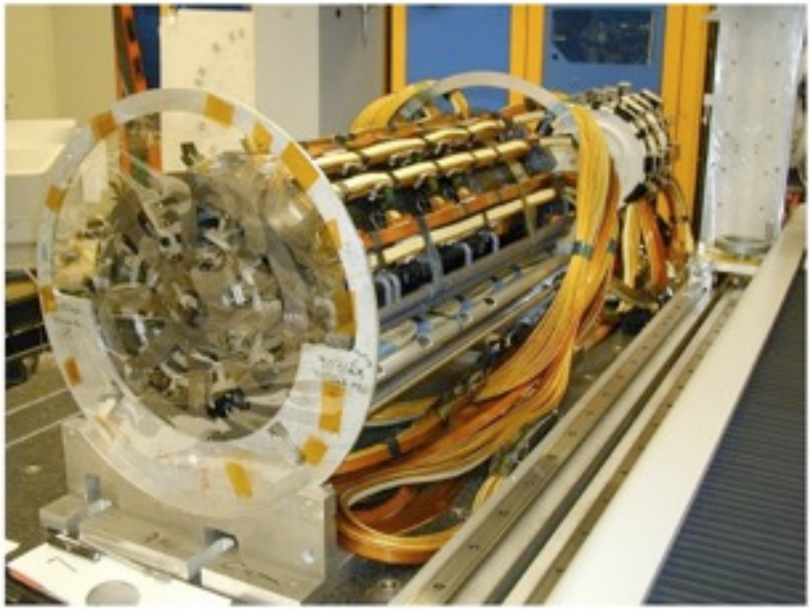
Subdividing simply the n+ contacts the presence of positive charge at the Si-SiO$_2$ interface induces in the n-type substrate an accumulation layer of electrons, resulting in a low resistance between the strips. Therefore the signal spreads over many electrodes, making the subdivision ineffective.



A method used to solve this problem is to implant a p+ blocking strip in between the n+ ones. The blocking strips are left floating, since their function is just to interrupt the conduction channel.

TEVATRON: D0



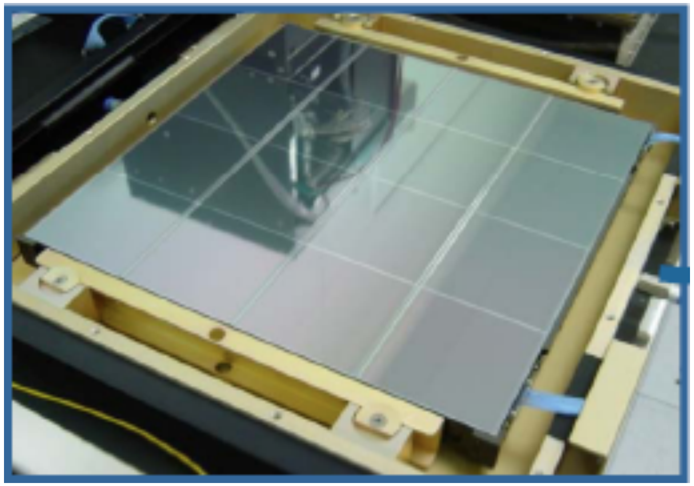


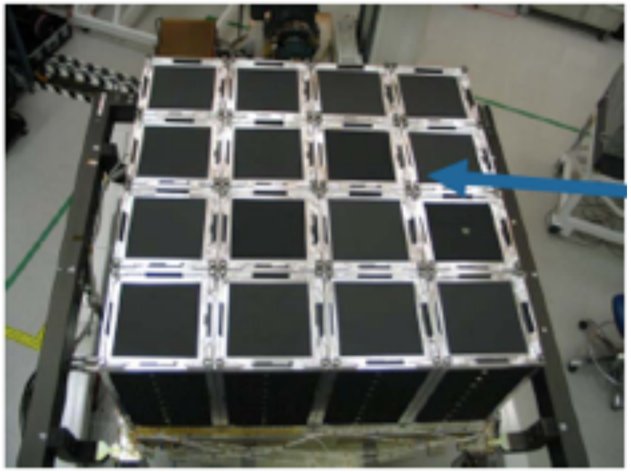
- Barrel and disc: strip detectors
- 840 k channels
- Operational since 2002

GLAST Mission

- 16 tower modules
- 37 × 37cm^2 active area
- 2 mm inter-tower separation to minimize the inactive area
- 70m^2 of Si (in space!!!)
- 11500 SSD 8.95X8.95 cm^2,
- 384 strips - 880,000 channels
  - 440 µm thick
  - 228 µm strip pitch

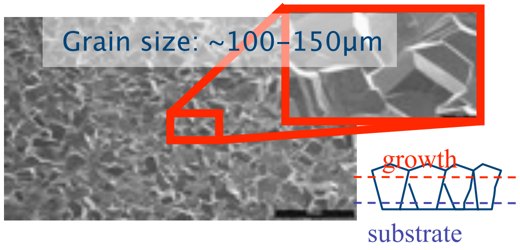
successfully launched 11. June 2008

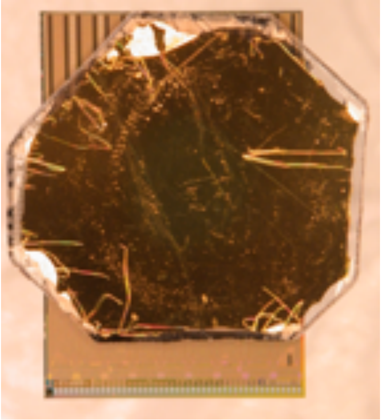




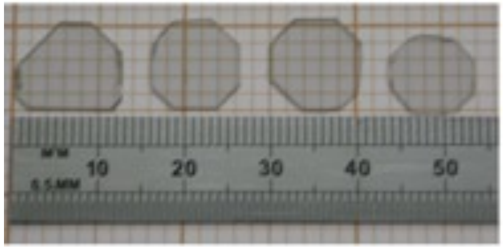
DIAMOND SENSOR

- Poly crystalline and single crystal
- Low leakage current, low noise
- Low capacitance
- Radiation hard material
- Operation at room temperature possible
- Drawback: 50% signal compared to silicon for same X_0
- But better S/N ratio (no dark current)

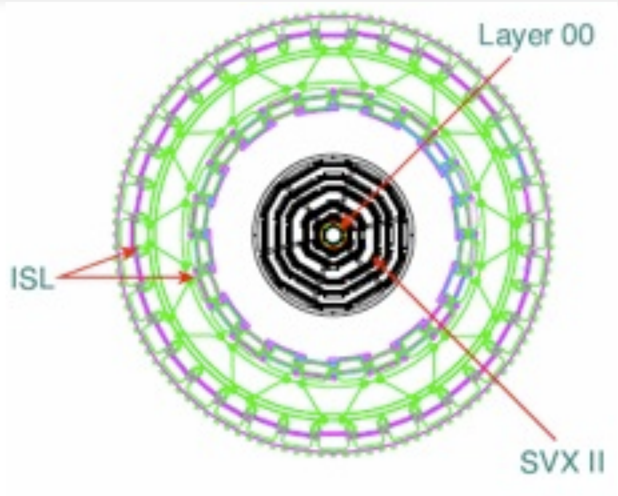


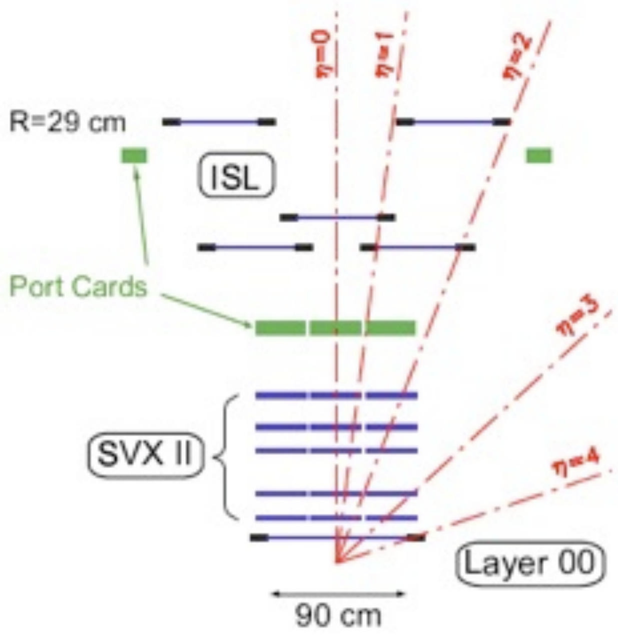


- Successful test of scCVD diamond pixel module
  - Stable operation
  - Full charge collection at 0.25 V/µm
  - Good efficiency: $\varepsilon > 99.9\%$
  - Measured Resolution: $\sigma = 8.9$ µm (200V, normal incidence)
- scCVD module retains ~80% of initial charge collected after irradiation to 0.7 x 10^{15} p/cm^2



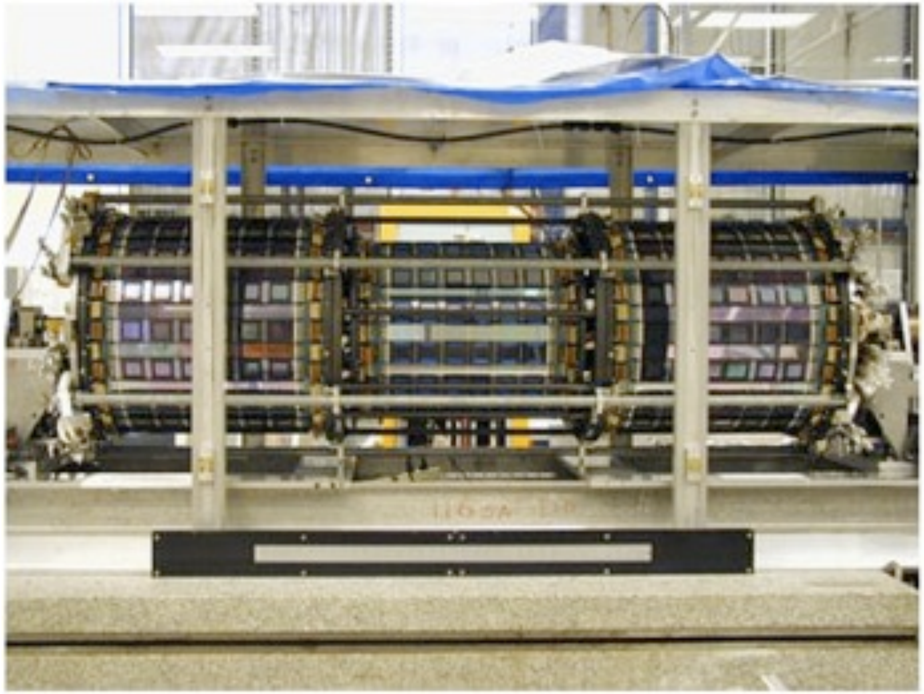
TEVATRON: CDF



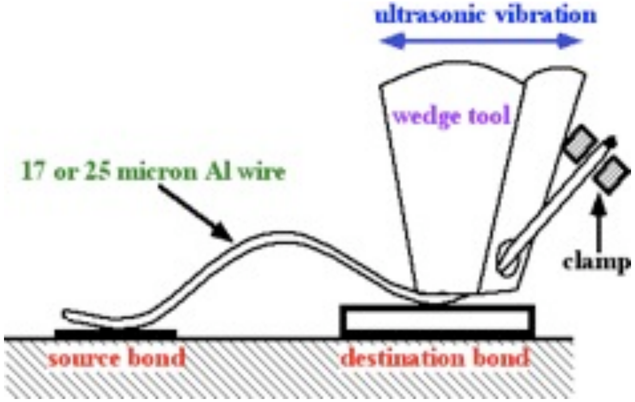


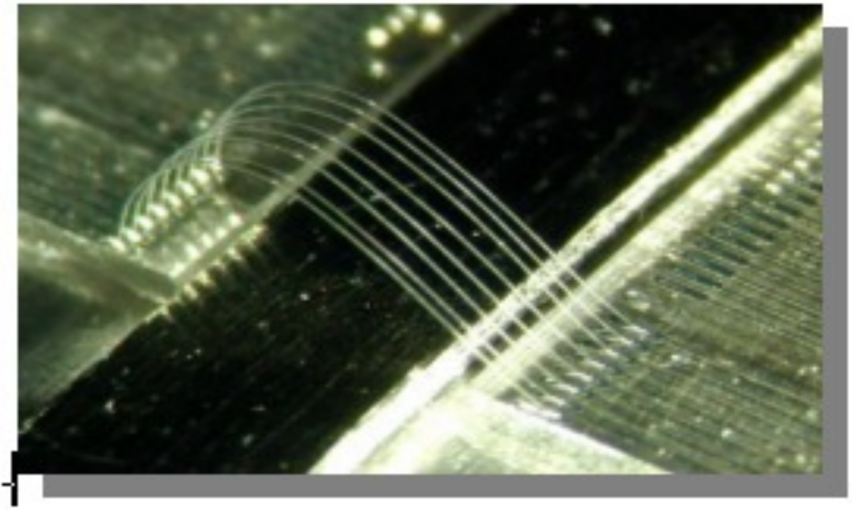
- Si-strip detector
  - special feature: Layer 00 directly on beam pipe
- 720 k channels
- Operational since 2002

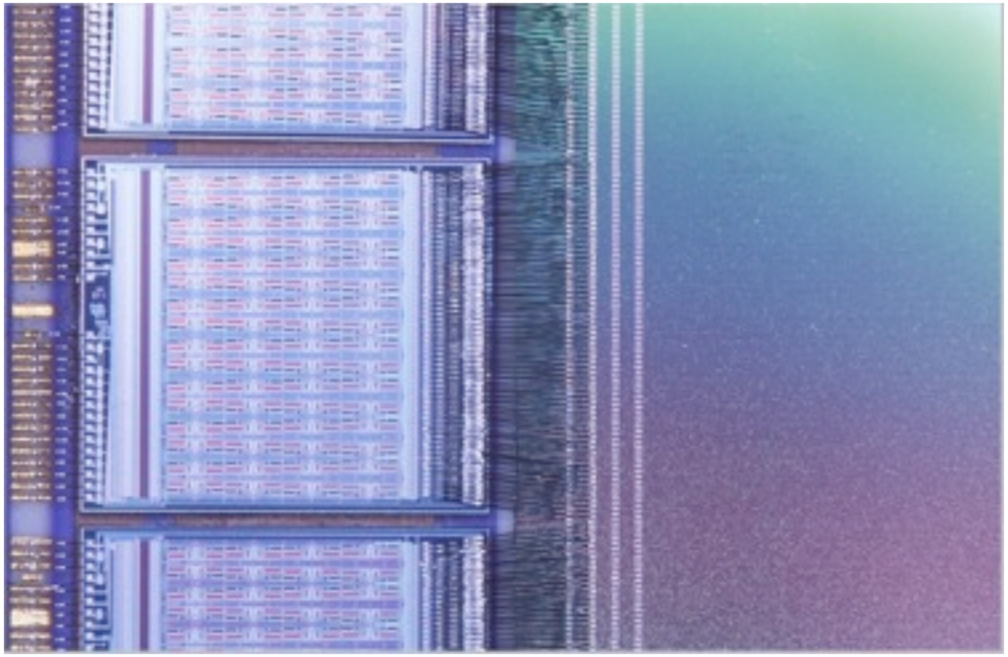
Inner Strip Layers (ISL):



BONDING


ultrasonic vibration
wedge tool
17 or 25 micron Al wire
clamp
source bond
destination bond





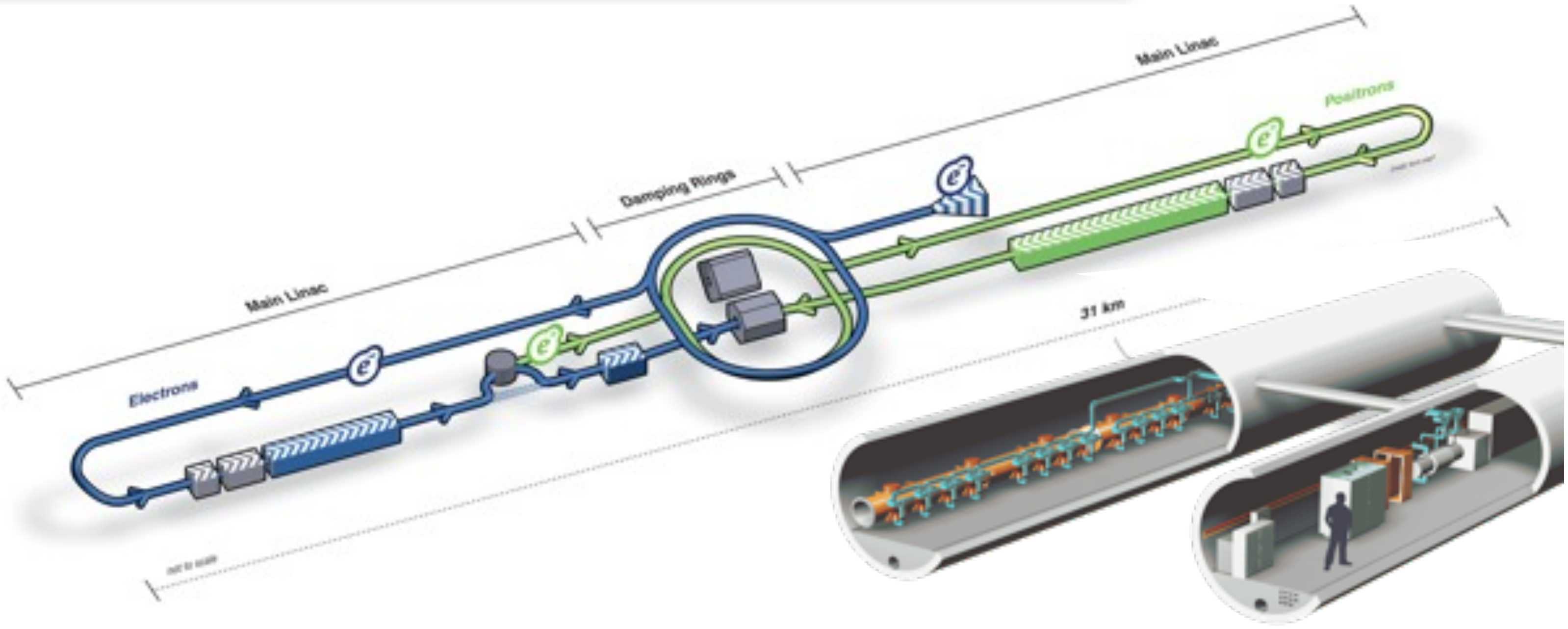
LARGE SCALE SILICON SYSTEMS

- The most critical parts are the sensors, ASICs and system engineering (mechanics, power, cooling, assembly, etc)

- To develop and buy silicon sensors for several hundreds of m^2 silicon sensors is not an easy task:

  - Extend previous Multi-Geometry studies to substrate thickness less than or equal the pitch
    - Strip/Pixel capacitance (back-plane, inter-strip/pixel & total)
    - Critical fields, depletion and break-down voltage
    - Sensor functionality (charge collection efficiency etc)
    - Detailed design parameters for masks
  - Extend previous studies from LHC to SLHC fluence – large irradiation programs needed
  - Extend previous studies to include n-on-p
  - Re-produce complementary sets of measurements and simulation
  - Study biasing, guard rings, isolation methods

THE INTERNATIONAL LINEAR COLLIDER



- e^--e^+ collider: two 11 km SC linacs at 31.5 MV/m
- Dual tunnel configuration (safety and accessibility)
- Single IR, crossing angle 14 mrad, two detectors in push-pull operation

Parameters:

- $\sqrt{s}$ = 500 GeV, tunable from 200 to 500 GeV, upgradeable to 1 TeV
- $\int L dt$ = 500 fb^{-1} in 4 years (peak luminosity $2 \cdot 10^{34}\, cm^{-2} s^{-1}$)