A new Clear Concept for DEPFET Active Pixel sensors

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430. WE-Heraeus-Seminar

Accelerators and Detectors at the Technology Frontier

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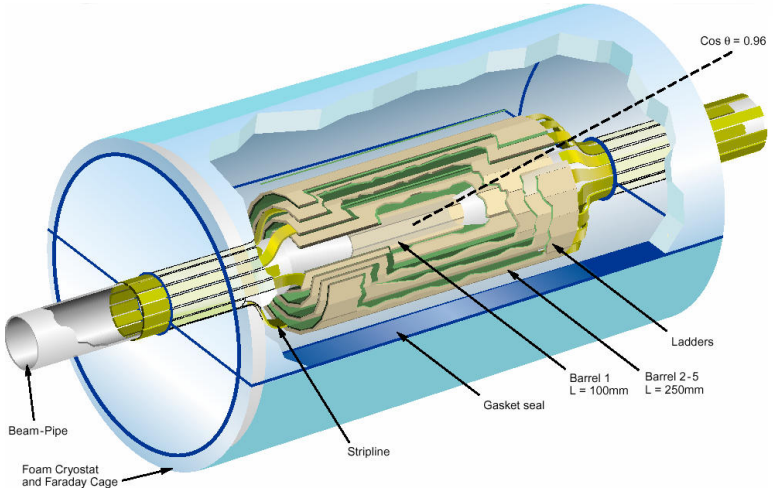
Overview

- DEPFET applications in HEP
- DEPFET principle
- The clear process
- Internal amplification
- The capacitive coupled Clear Gate

DEPFET application in HEP

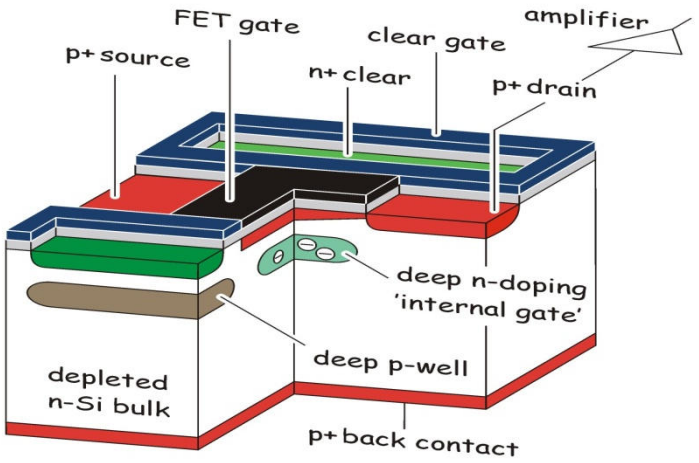
- Applications:
  - Vertex detector at ILC
  - Vertex detector at SBelle



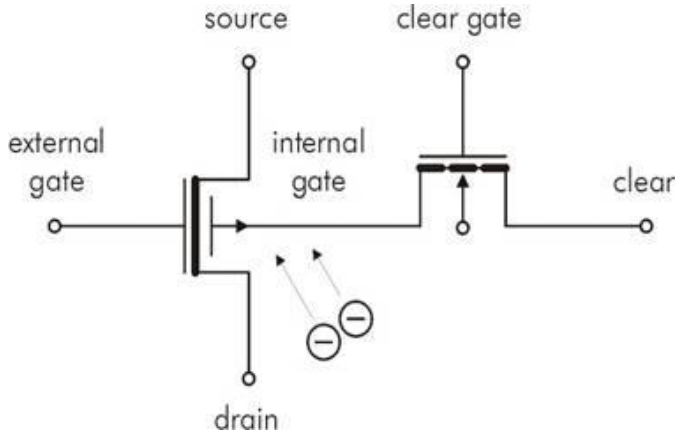
- Requirements:
  - Good point resolution ILC: 24µm SBelle ~50µm
  - Small material budget ~0.1 % X_0 per layer
  - High readout rate: Frame rate ~ 20kHz (100kHz) ~50-100ns/Row
  - Radiation hardness 100kRad/~1MRad

DEPFET – Depleted Field Effect Transistor

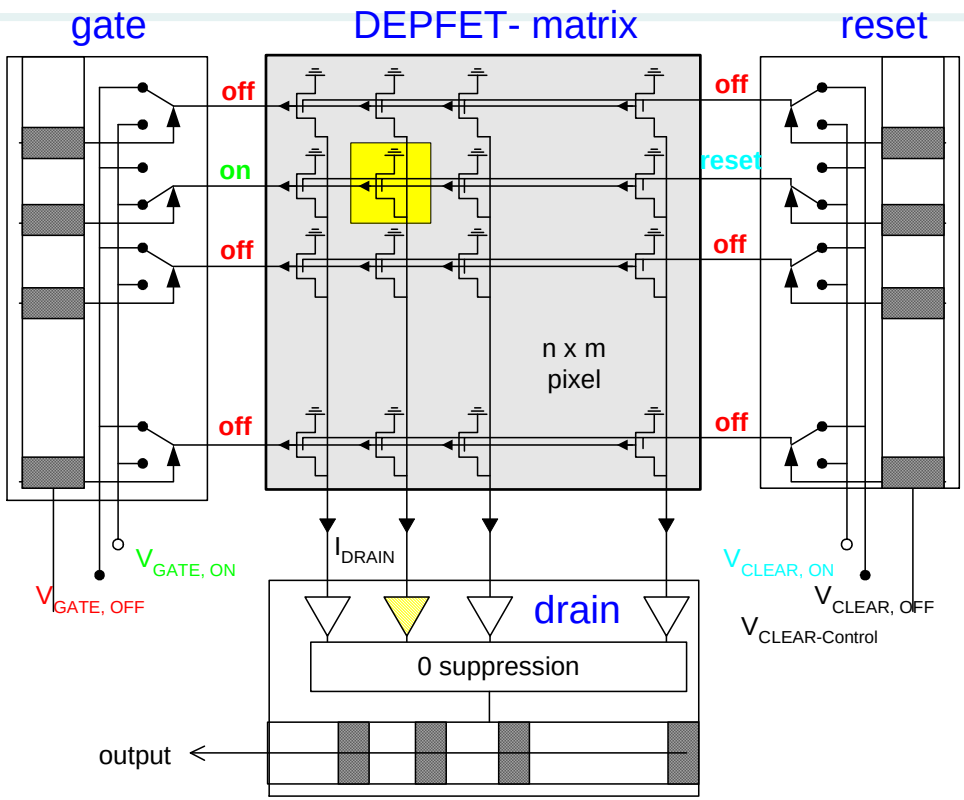
- Combination of detector grade silicon with first **p-FET** amplification stage in each pixel
- **Potential minimum for electrons** is created under the channel by **sideward depletion** and an additional **n-doping**
- Electrons in the "internal gate" **modulate the transistor current**
- Signal charge is removed via a clear contact

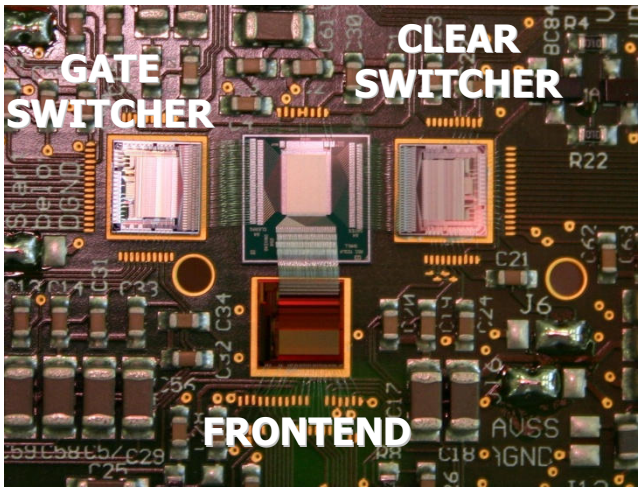


- **Large sensitive volume** due to **fully depleted** bulk
- **Low noise** caused by a small input capacitance and **internal amplification**
- Transistor can be **switched off** by external gate – charge collection is then still active!



DEPFET – Matrix operation



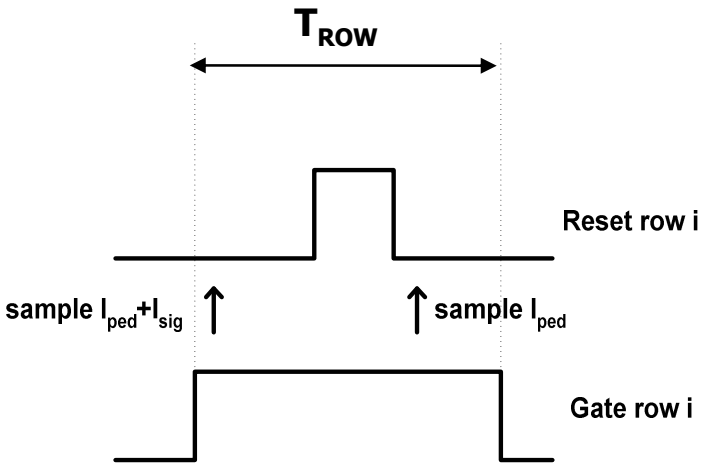


- Column parallel architecture for fast readout
- Local charge to current conversion – no charge transfer
- Low power dissipation – only one row active while readout

Readout sequence

- Gates are connected row wise
- Drains are connected column wise
- Sample – Clear – Sample
- Difference of two consecutive samples:

I_{SIG} = Sample 1 – Sample 2 = $(I_{PED} + I_{SIG}) - I_{PED}$



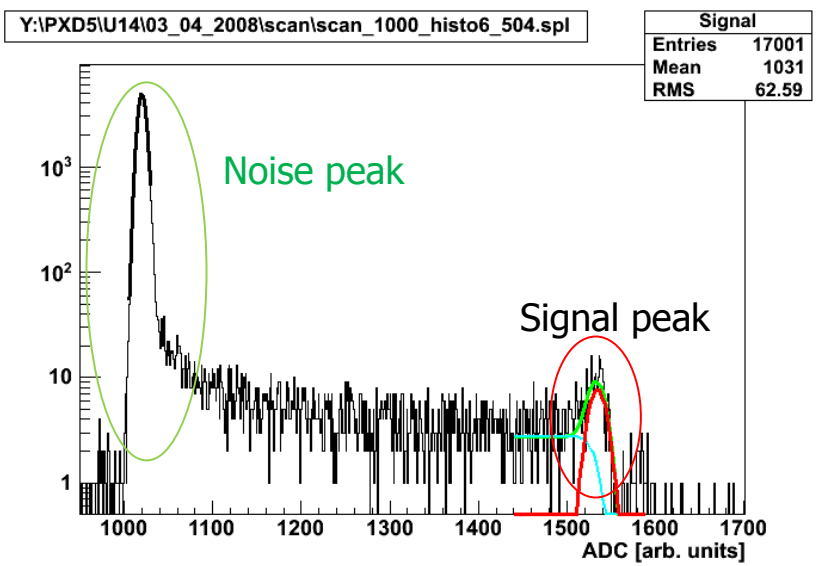
- DEPFET operation relies on:

  - Clear process
  - Internal amplification
  - And others…

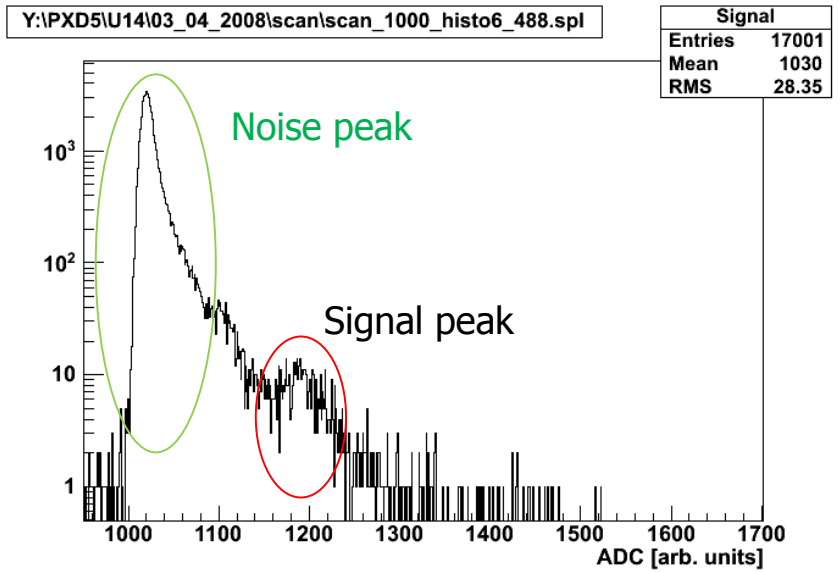
The clear process

Clear- and system performance

Full clear:



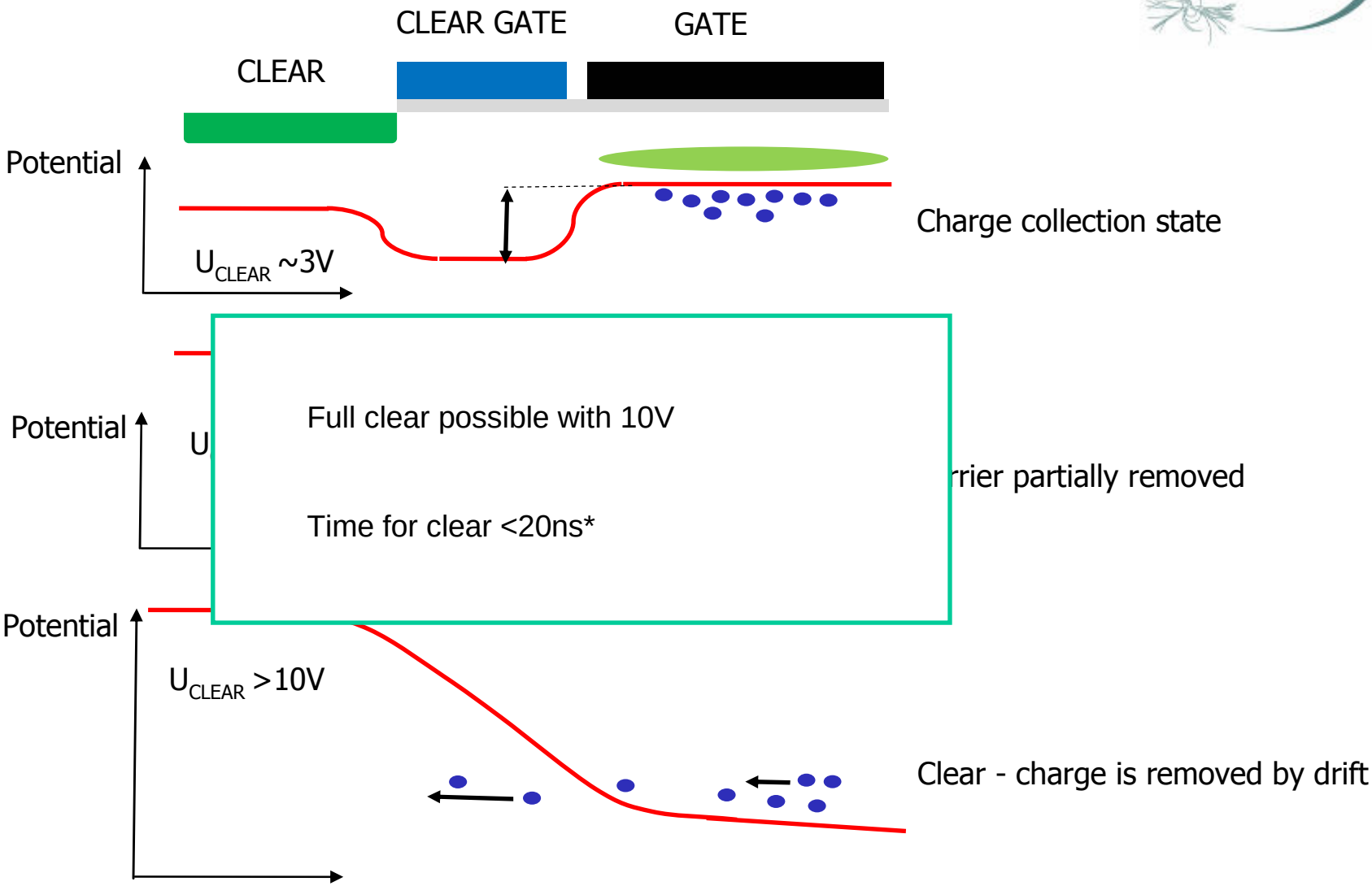
Incomplete clear:



Incomplete clear causes:

- Loss of signal pulse height: $I_{SIG} = (I_{PED} + I_{SIG}) - (I_{PED} + I_{REM})$
- Increase of noise

The clear process



* [C. Sandow and others; NIM A 2006,176-180]

Internal amplification

Internal amplification

- Charge to current conversion gain: $g_q = dI_{ds}/dQ_{int}$
- Determines the signal: $I_{sig} = g_q * Q$ (Q ~ 4000e for 50µm Si)
- In presence of external noise SNR ~ g_q

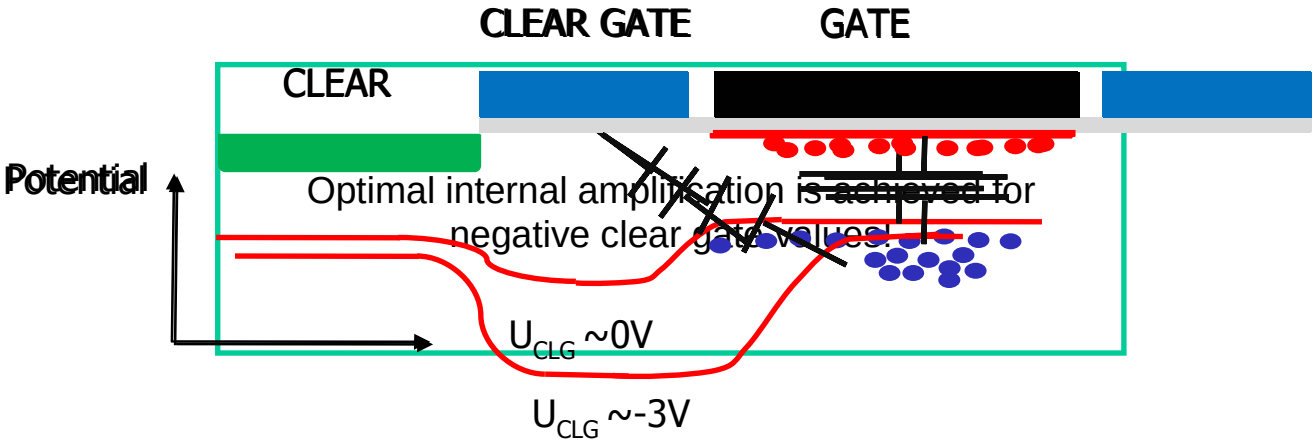
- It depends on the
  - Geometry of the FET
  - Current
  - **Clear Gate voltage**

Standard devices: ~ 350pA/e^-

Up to 1400pA/e^- demonstrated

Gain modulation with Clear Gate

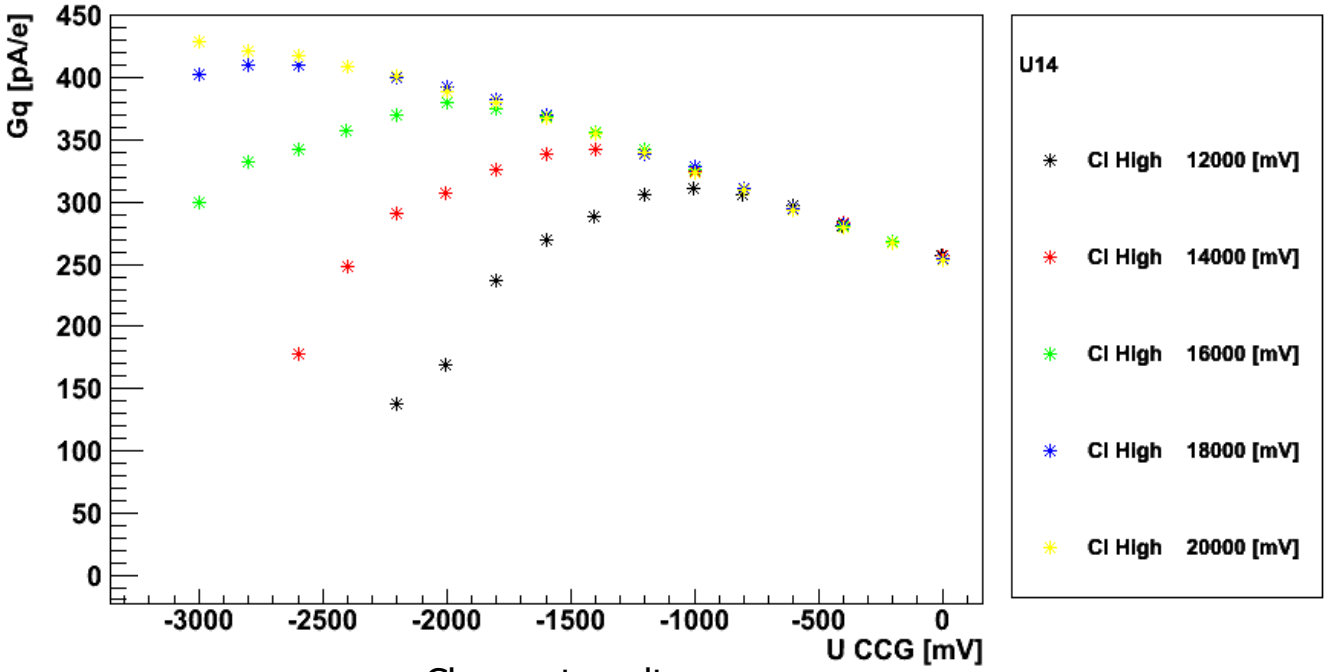
- Dependence of internal amplification on Clear Gate voltage
- Reduction of parasitic capacitances



Optimal operation point

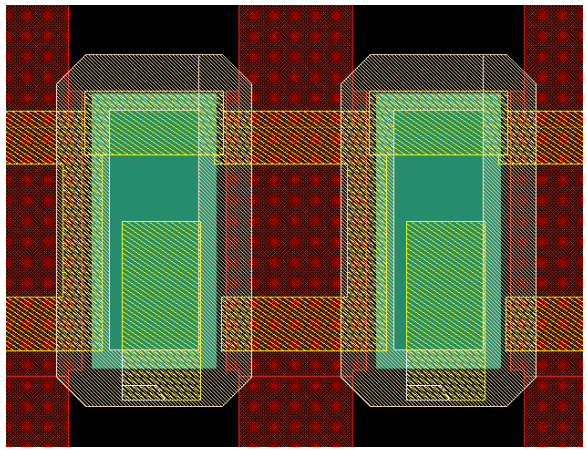
- Full clear - low Clear Gate voltage
- High internal amplification - high Clear Gate voltage

- Tradeoff neccesary!



Clear gate voltage

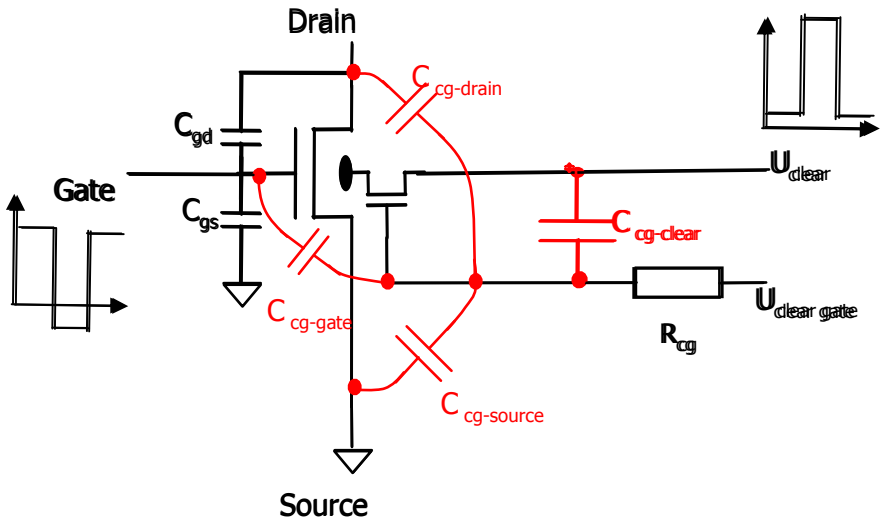
The capacitive coupled Clear Gate



- Reducing the potential barrier via build in capacitor
- DC potential defined by resistor
- Potential change given by:

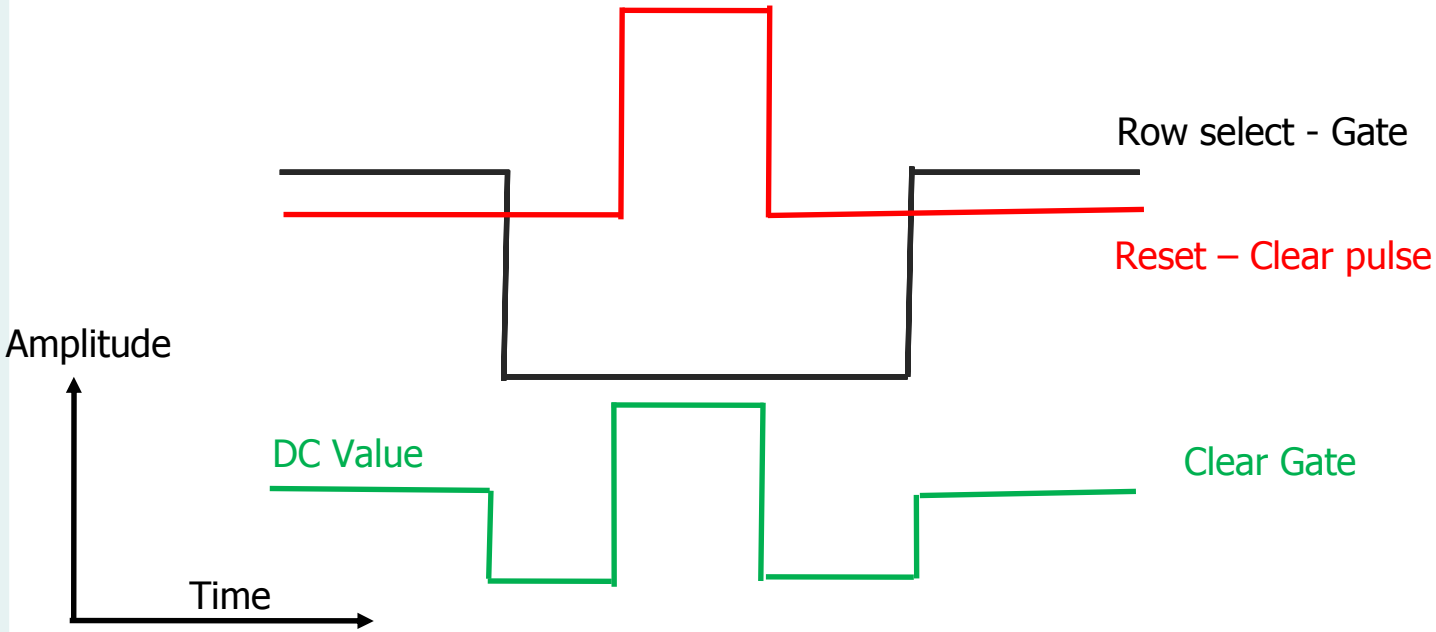
$$\delta U_{clg} = \frac{C_{clg-clear}}{C_{tot}} \cdot \Delta U_{clear} + \frac{C_{clg-gate}}{C_{tot}} \cdot \Delta U_{gate}$$

(capacitive voltage divider)



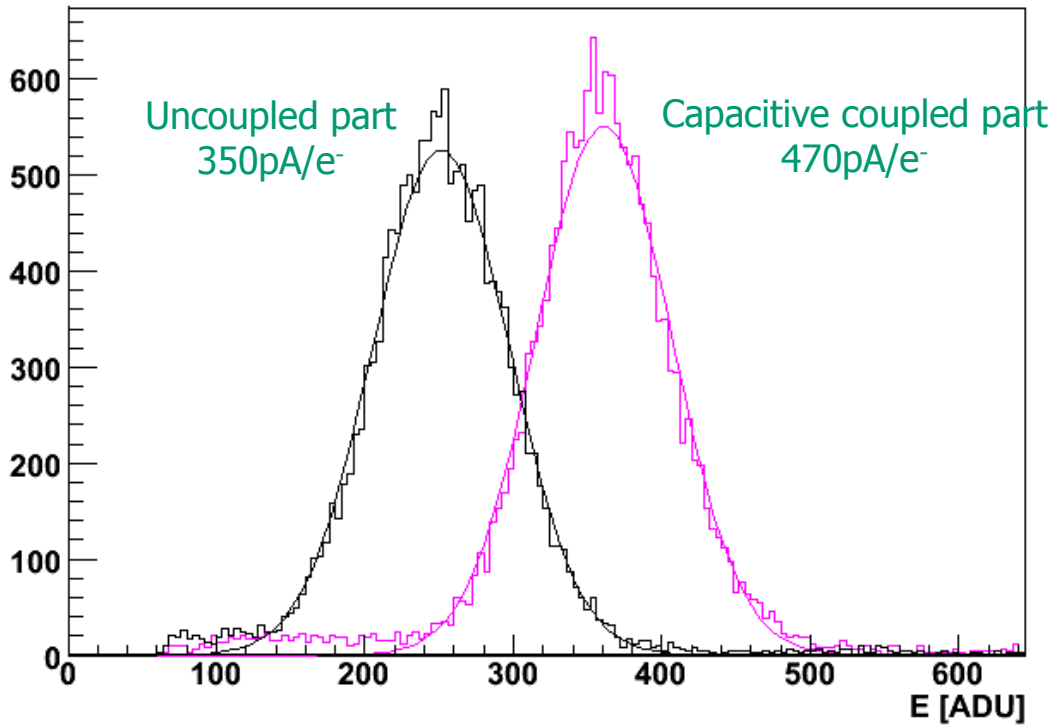
Coupling

- Both parasitic and intended coupling could be extracted from layout:
  - Clear Gate – Clear: ~210mV/V
  - Clear Gate – Gate: ~160mV/V
- Typically voltage swing of Clear and Gate are similar ~ 10V



- Twofold improvement:
  - Clear Gate is lowered when row select is applied
  - Clear Gate is increased when reset pulse is applied

Demonstration with Cd^{122} spectrum



Cd^{122} : X-ray @ 22keV

128 x 64 Pixel matrix

Spectrum taken
after optimization

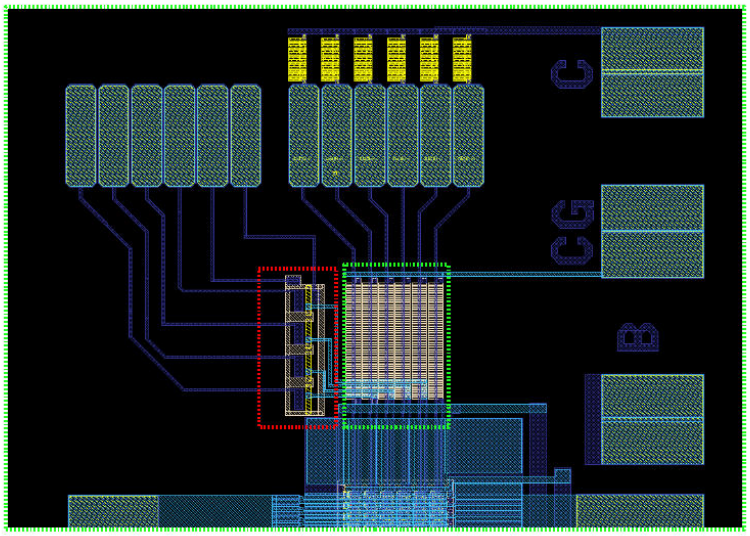
- Internal amplification significantly improved to 470 pA/e^- !
  @ 10V clear voltage swing

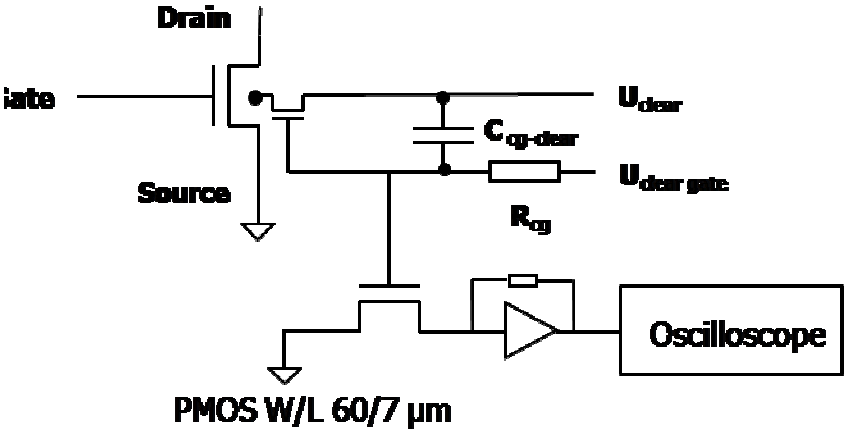
Summary

- The capacitive coupled Clear Gate scheme is working
- The internal amplification is significantly improved – 470pA/e^- - with a voltage swing of 10V on the clear!
- The readout noise is reduced by 35%!

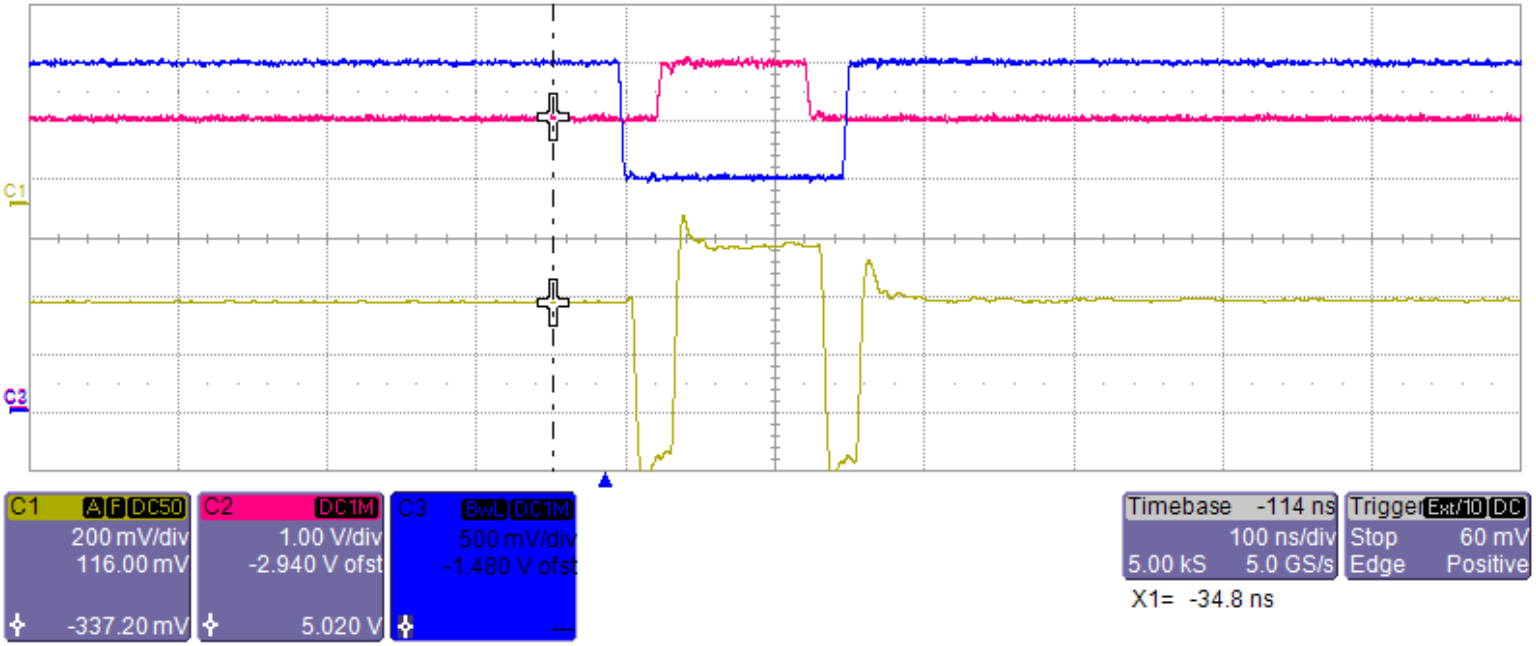
Direct measurement of the coupling

- Direct measurement possible with test structure with additional transistor

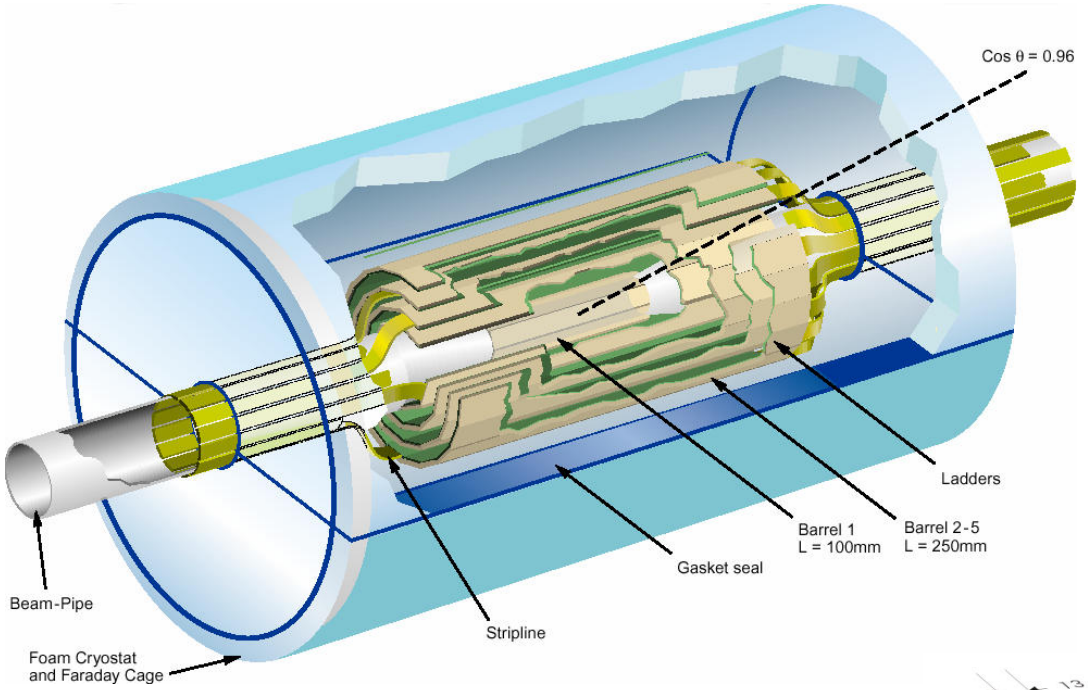


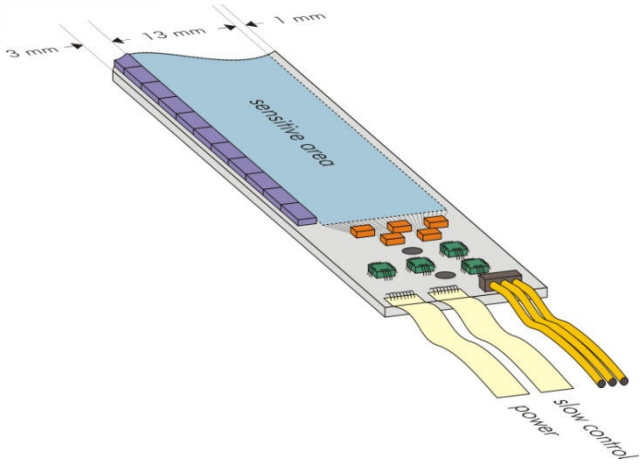


Direct measurement

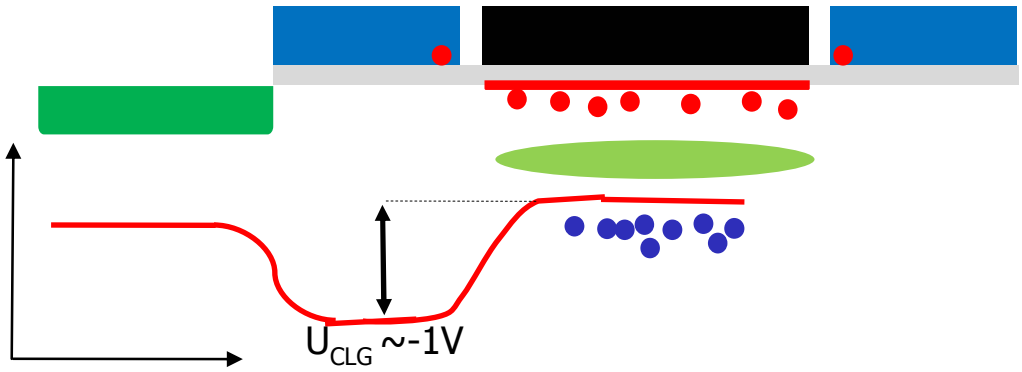


DEPFET as vertex detector for ILC





- IP resolution: $\sigma_d \leq 5\mu m \oplus \frac{10\mu m}{p \cdot \sin^{3/2}\vartheta} \frac{GeV}{c}$ [Tesla TDR]
  - Excellent point resolution
  - Small material budget 0.1 % X_0 per layer
- Frame rate ~ 20kHz ~50-100ns/Row
- Sufficient radiation hardness


U_{CLG} ~-1V